The CMS ECAL Upgrade for High Precision Timing and Energy Measurements in HL-LHC

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Phase II: High Luminosity LHC

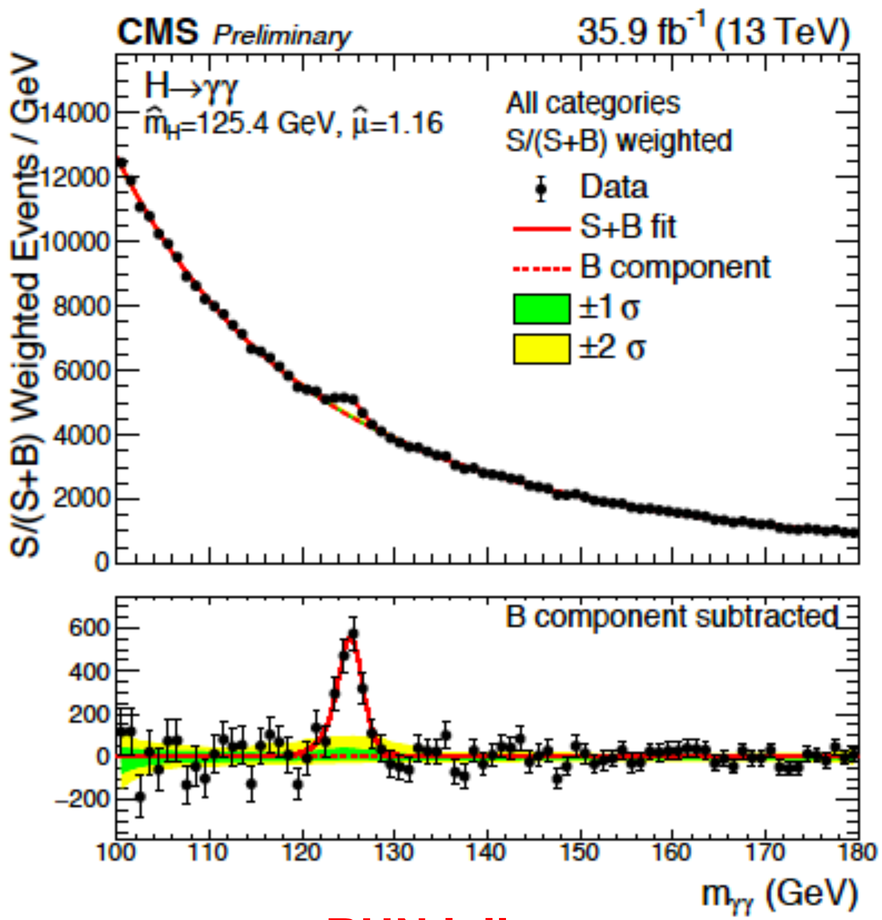
- ❑ HL-LHC: expected to deliver 10x the luminosity delivered in Phase I

	LHC	HL-LHC baseline	HL-LHC ultimate*
$\mathcal{L}_{inst}(\mathrm{cm}^{-2}\mathrm{s}^{-1})$	2×10^{34}	5×10^{34}	7.5×10^{34}
PU (n_{vtxs})	40-60	140	200

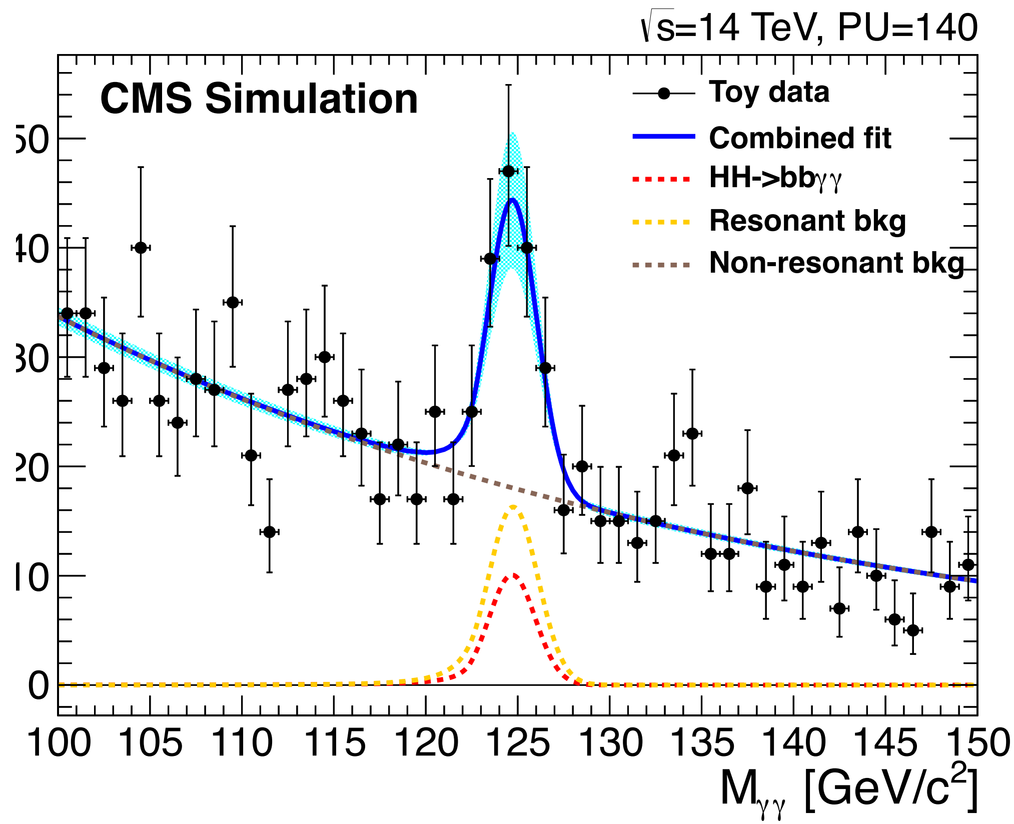
*unexpected at the time of original ECAL TDR.

- ❑ CMS upgrade
  - Increased acceptance: tracker (|η|=4) and muon spectrometer (|η|=2.8)
  - Higher first level trigger (L1) rate: 100kHz → 750kHz
    - ➢ to maintain comparable trigger performance at higher pileup
  - L1 trigger latency 3.4μs → 12.5μs
    - ➢ to provide time for the new track-based hardware trigger

EM energy resolution and Higgs



RUN I, II



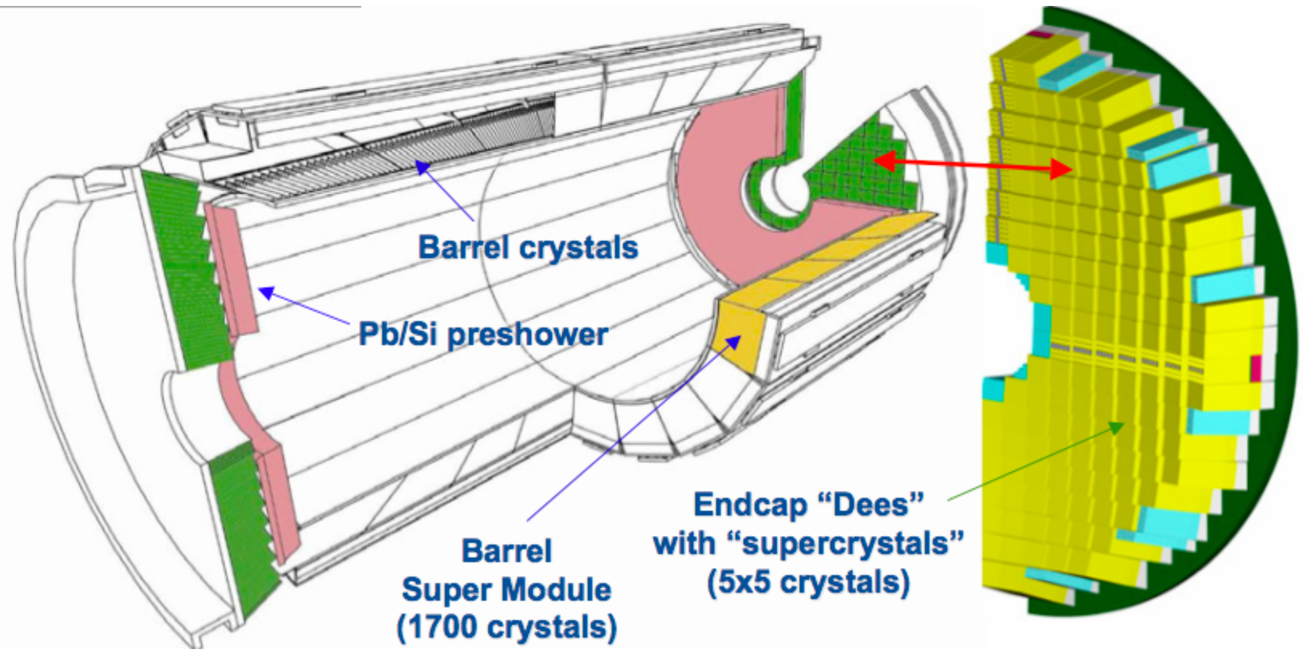
CMS-PAS-FTR-15-002

HL-LHC

- Discovery and inclusive properties
- First determination of couplings and differential properties
- $m_{\gamma\gamma}$ resolution ~1%

- One of the main goals:
  Discovery of di-Higgs HH production
- Higgs Boson self coupling

ECAL: from Phase 1 to HL-LHC



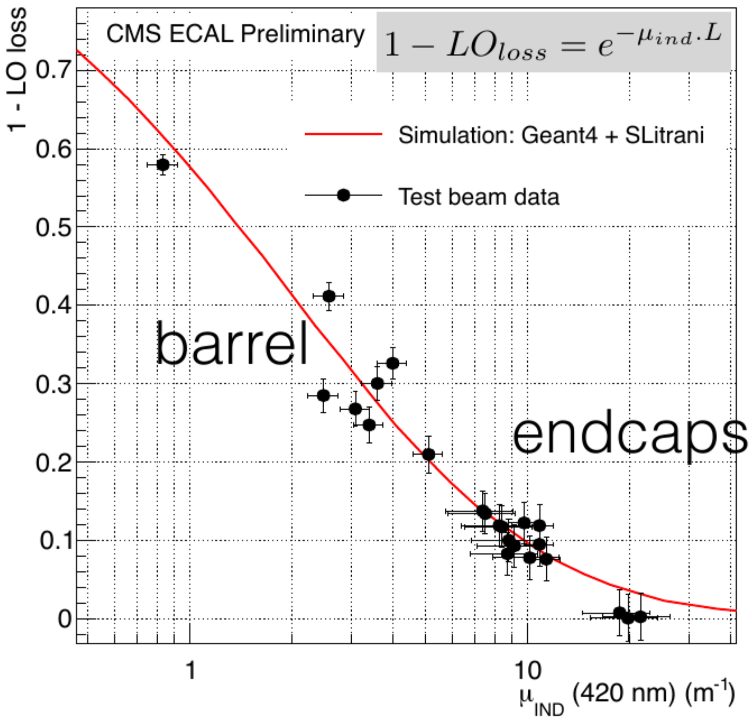
Barrel (EB)
$|\eta| < 1.48$
61200 crystals
Avalanche Photo-Diode (APD) readout

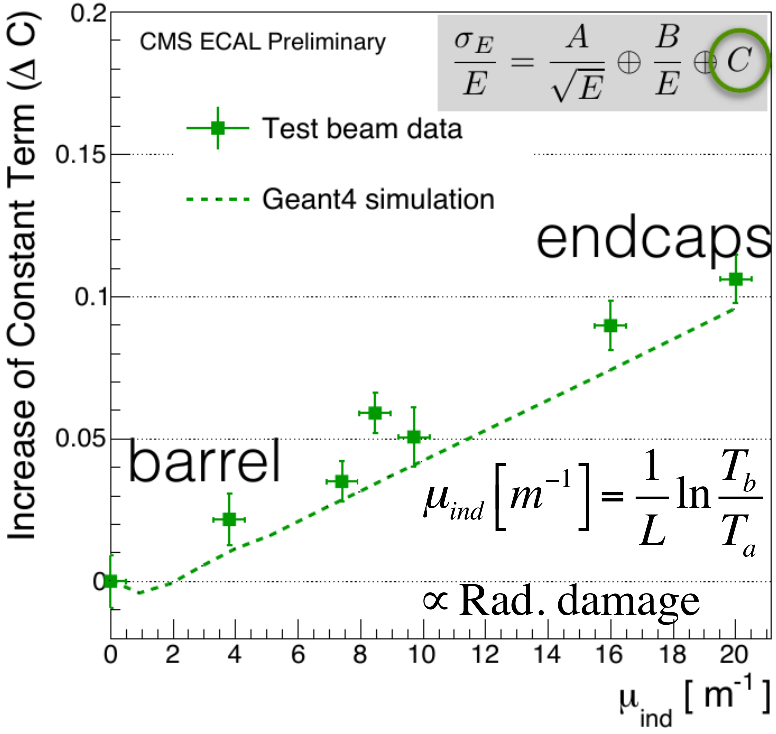
Endcaps (EE)
$1.48 < |\eta| < 3.0$
14648 crystals
Vacuum Photo-Triode (VPT) readout

Pb/Si preshower
$1.65 < |\eta| < 2.6$
3X0 of Pb/Si Strips

- Endcaps: complete replacement of current calorimeters to cope with expected radiation flux
  - ✓ HGCAL: High Granularity (Silicon-based) Sampling Calorimeter
- Barrel:
  - ✓ ECAL: retain crystals+APD → upgraded readout electronics
  - ✓ HCAL: Brass/plastic scintillator + SiPM

ECAL resolution at HL-LHC





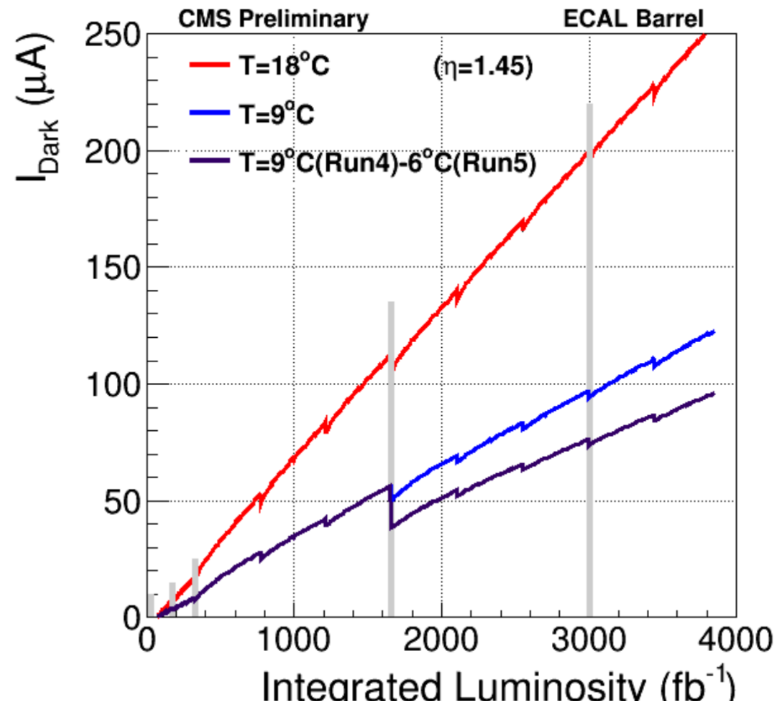
- Barrel: crystals will retain 30-50% of light output after 3000fb^{-1}
- Endcaps: crystals lose most of the light output.

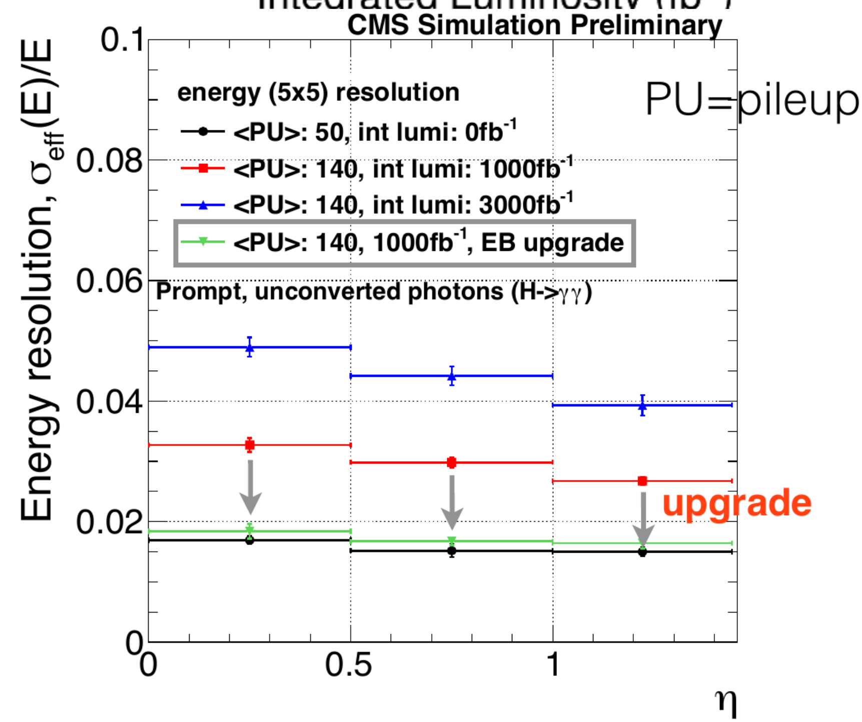
- Constant term for Barrel acceptable.
- Constant term for Endcaps ~10%, leads to unacceptable energy resolution.

ECAL APD performance

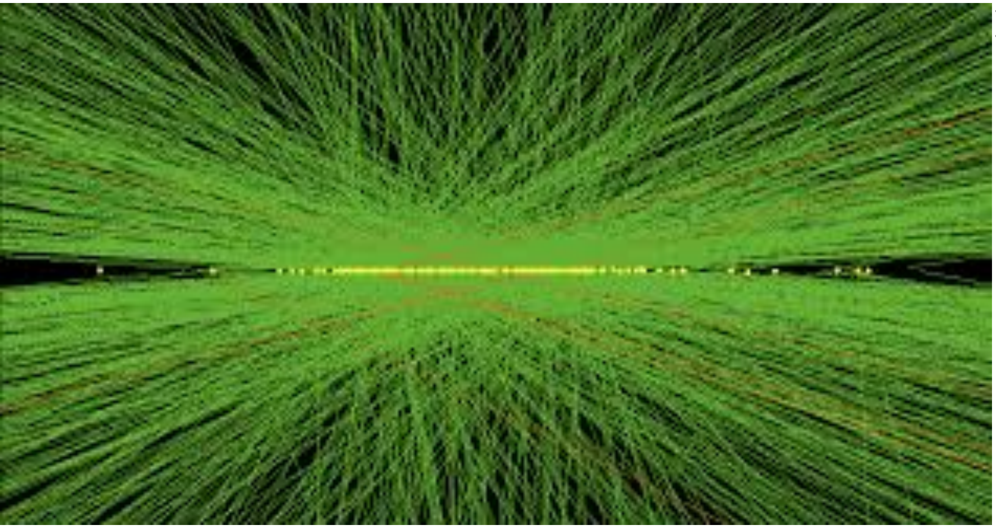
- ECAL APDs will continue to operate well during HL-LHC
  - Increase in leakage current due to radiation damage
    - APD noise will dominate energy resolution at HL-LHC

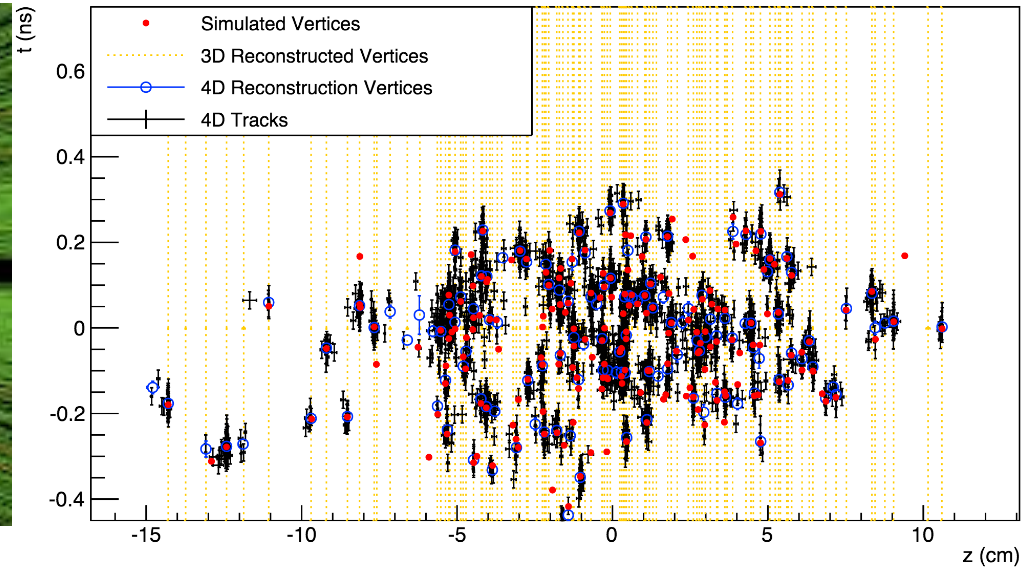
- Actions Taken:
  - ✓ Lower ECAL operation temperature from 18°C to 6-9°C
  - ✓ To reduce the PU impact and obtain better S/N, the pre-amplifier will have shorter signal pulse length.



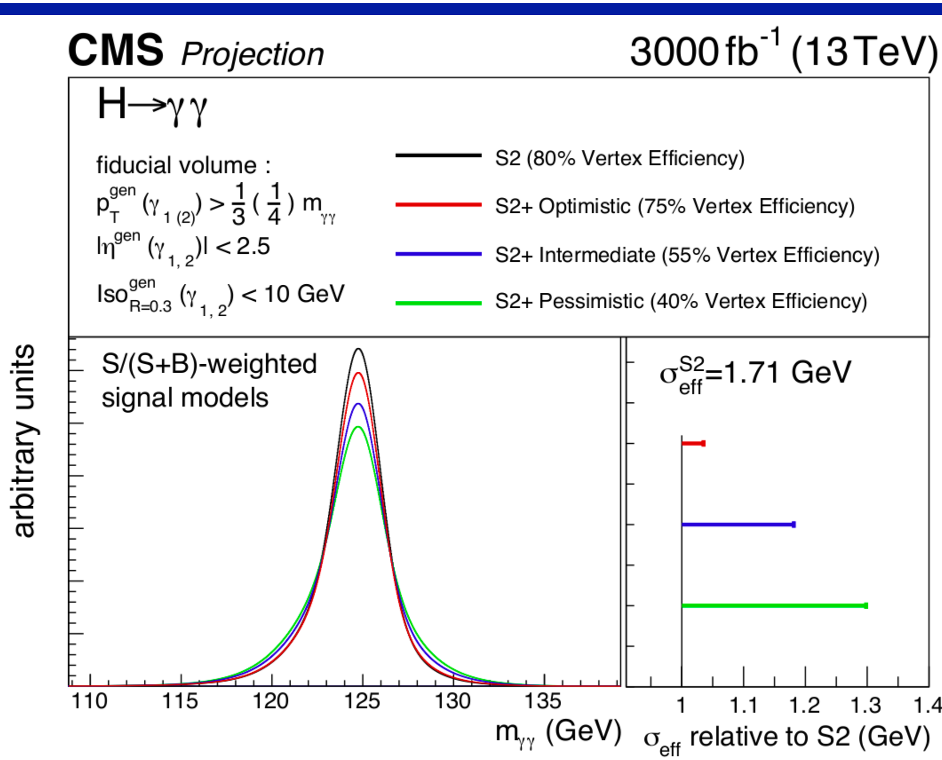


PU: Timing Resolution



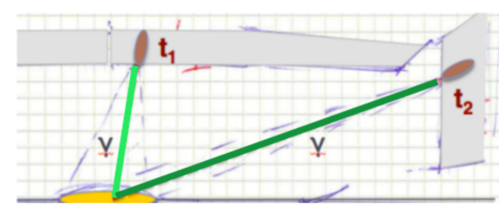


Phase II Pileup 5x higher than Phase I
Vertex ID efficiency drops from 80% to 40%



- Precise ~30ps TOF timing can improve vtx ID
- $PbWO_4$+APD intrinsic resolution <30ps
- Global CMS effort to provide high precision clock

H→γγ mass Resolution under different assumptions



No precise timing
+ upgraded ECAL timing
+ new CMS MIP timing layer

ECAL Challenges at Phase II

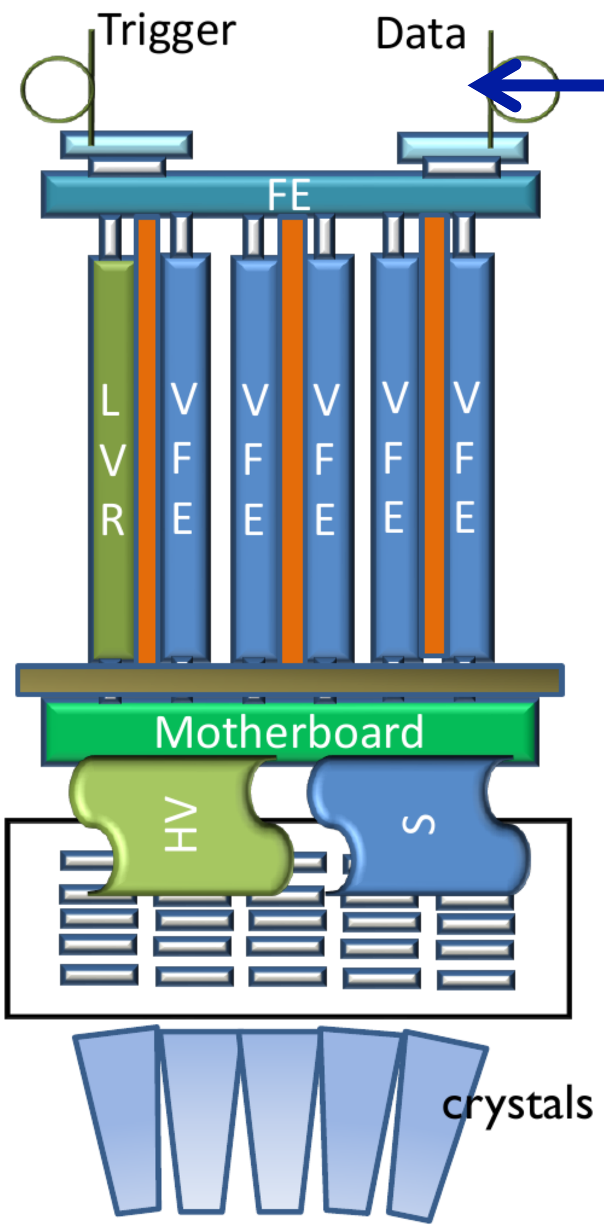
Phase II goal:

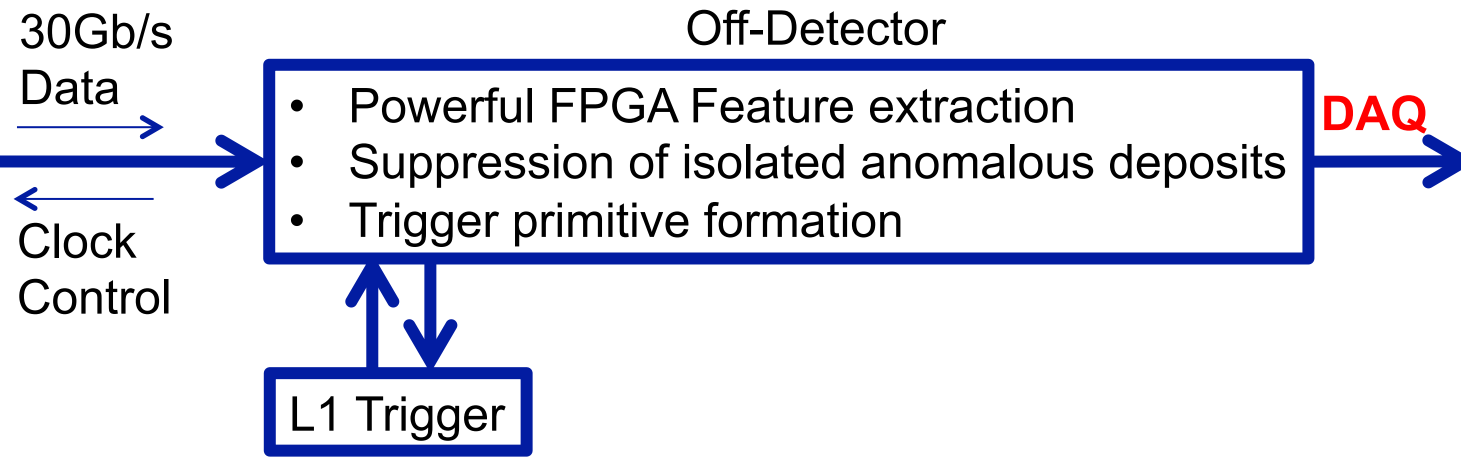
- ❑ Preserve current ECAL physics performance under HL-LHC and CMS Phase II conditions and demands

Challenges:

- ❑ Higher trigger rates and longer latency
- ❑ Crystal transparency loss due to higher radiation damage
  - ✓ Impacts ECAL energy resolution
- ❑ 10x noise increase from APD leakage currents due to higher radiation damage
  - ✓ Dominates ECAL energy resolution
- ❑ Reduced vertex ID efficiency due to much higher pileup
  - ✓ Impacts $H \rightarrow \gamma\gamma$ mass resolution
- ❑ Increased pileup contamination
  - ✓ Impacts ECAL energy resolution

ECAL Upgrade





Main Reason: cope with higher L1 trigger rate and latency

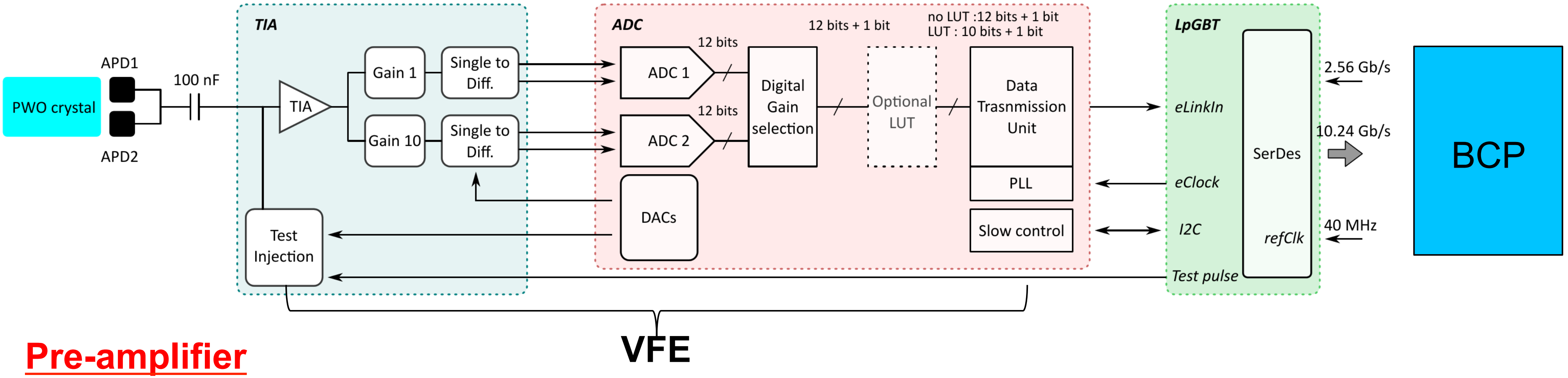
Replace VFE and FE:

- Stream detector data along one path.
- Move pipelines and trigger primitive generation to off-detector

Re-design VFE:

- Reduce shaping time
- Increase sampling frequency (160MHz)
- New ADC and data compression
  - ✓ Excellent energy resolution
  - ✓ Fast response for pileup mitigation and noise reduction
  - ✓ Timing resolution and spike discrimination

ECAL upgraded electronics



Pre-amplifier

- Trans Impedance Amp (TIA) architecture optimizes pulse length and sampling rate.
- Matches the requirements for noise, spike rejection, pileup mitigation, and precision timing.
- 2 TeV dynamic range, two gain ranges (G1, G10) with 50, 500 MeV LSB

ADC

- 12 bit, 160MHz sampling frequency
- IP block which will be put in custom chip with rad hard design + data compression in Data TU

FE

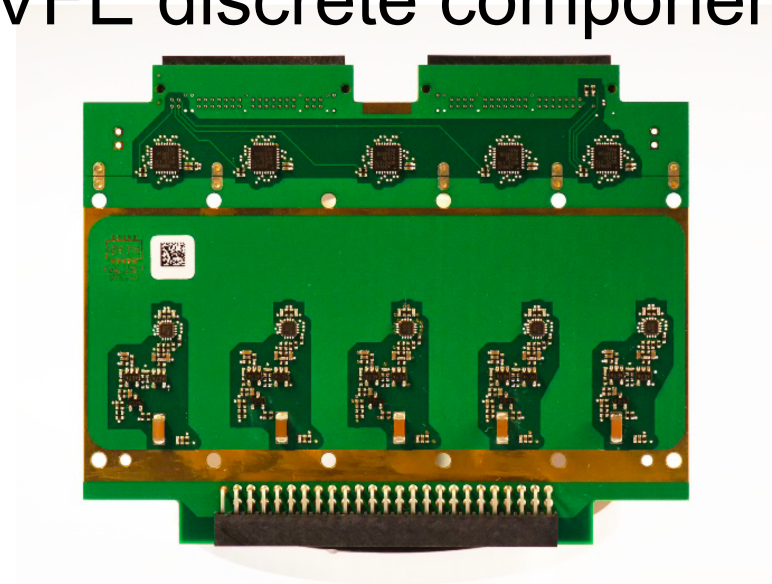
- Fast rad-hard optical links to stream crystal data off-detector (OD) through CERN lpGBT/VL

BCP

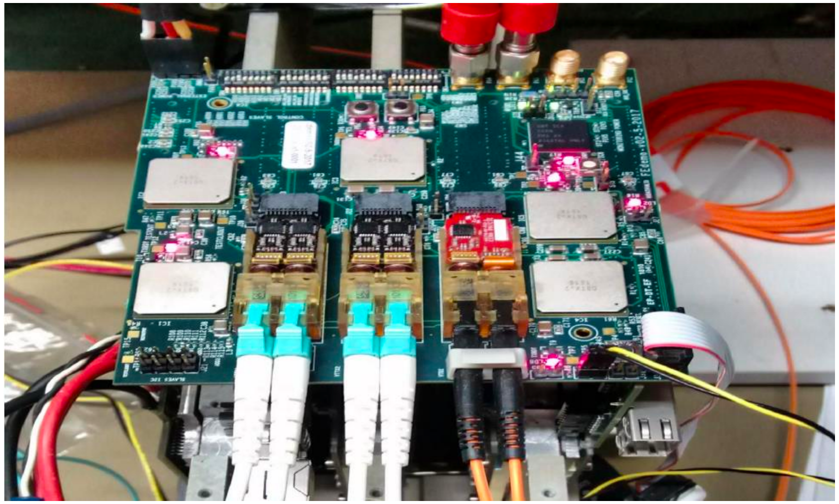
- Barrel calorimeter processor, FPGA based → Data pipeline, trigger primitives, signal analysis for spike reduction, channel calibration and more

Some Hardware

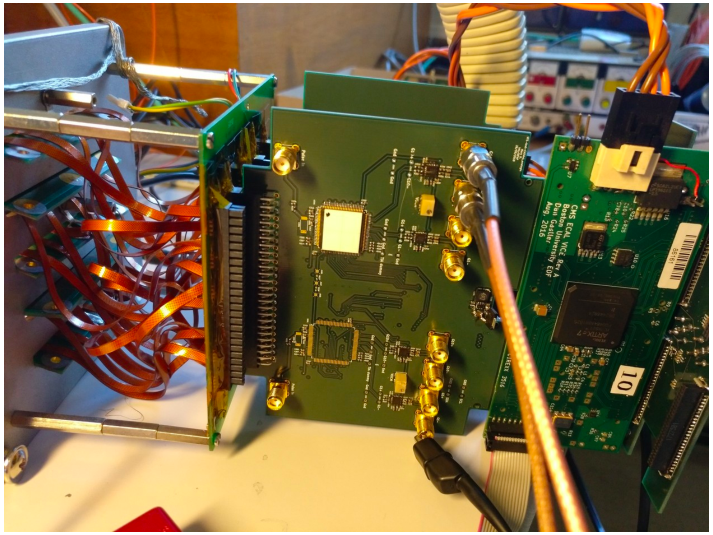
VFE discrete components



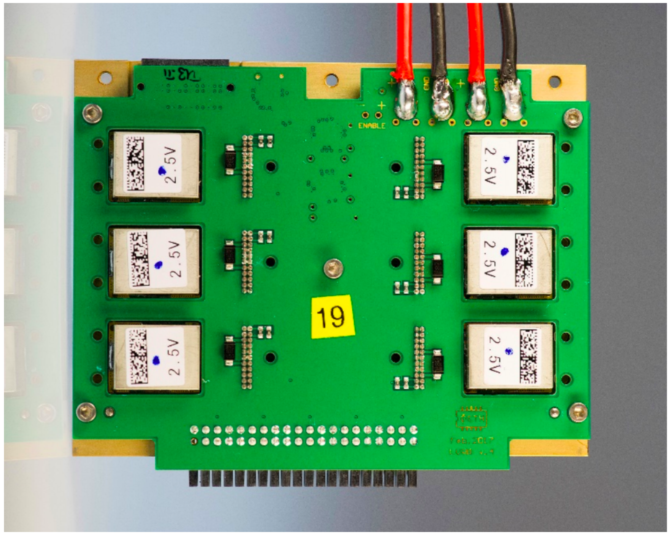
FE prototype



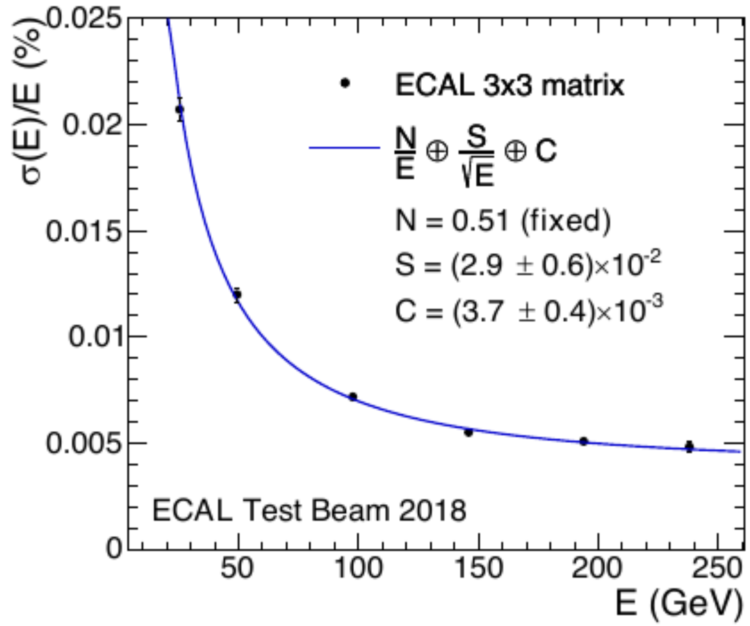
CATIA asic analog board



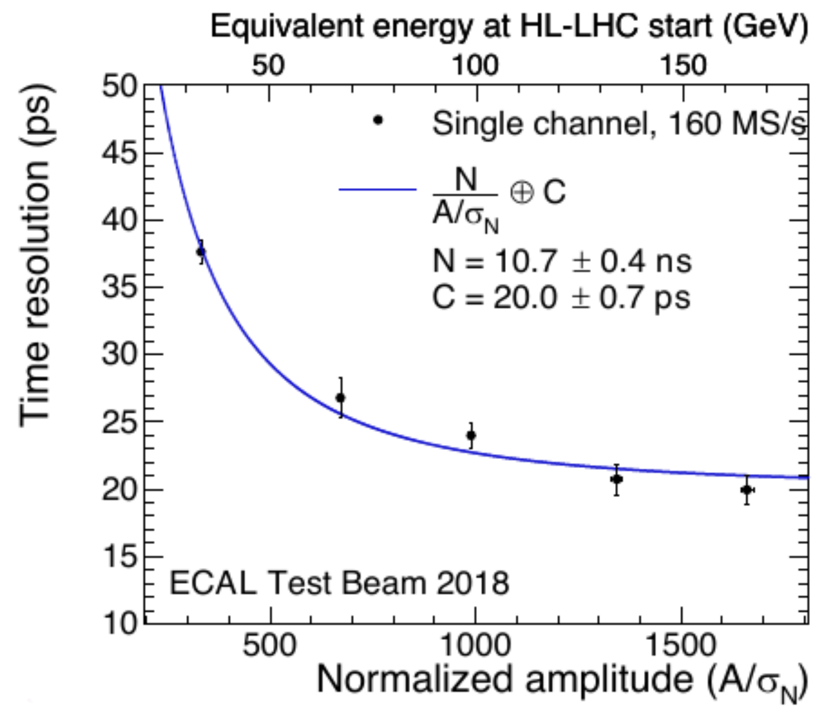
Low voltage regulator prototype



VFE prototypes in 2018 Test Beam



Energy Resolution:
matches CMS phase I



Time Resolution:
Matches target of <30ps for E>50GeV

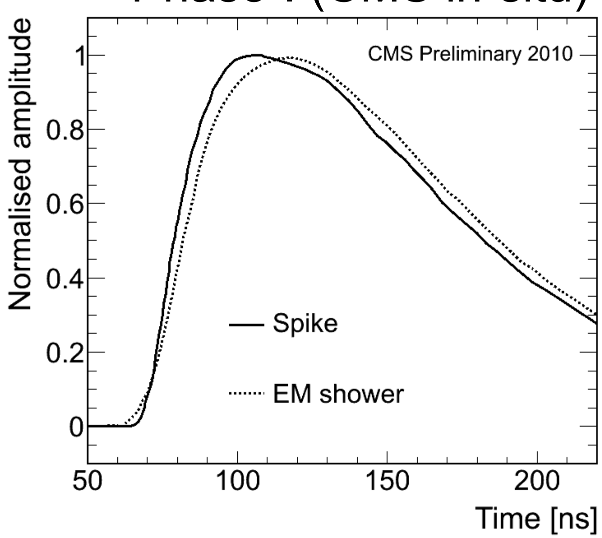
- ❑ One ECAL tower (5x5=25 channels) equipped with the first prototype of Phase II ASIC amplification chip and 160 MHz commercial ADC
- ❑ Electron beam: 25-250 GeV energy range. Setup kept at 18^{o}C

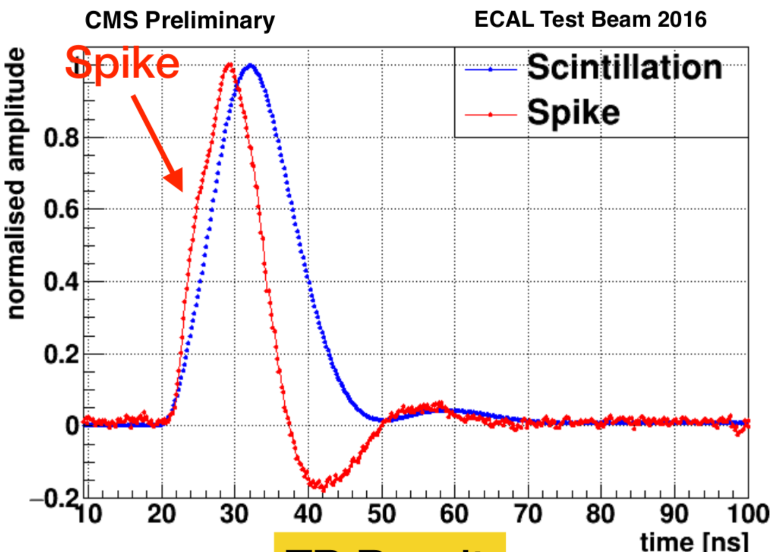
Trigger

- ❑ Granularity increase from tower level (5x5) to crystal level
- ❑ More sophisticated hardware-level trigger algorithms
- ❑ Pileup and background rejection
- ❑ Online signal shape analysis → online reduction of anomalous hadron signals.
  - ✓ Target: 1kHz for E > 5GeV

CMS-DP-2012/008

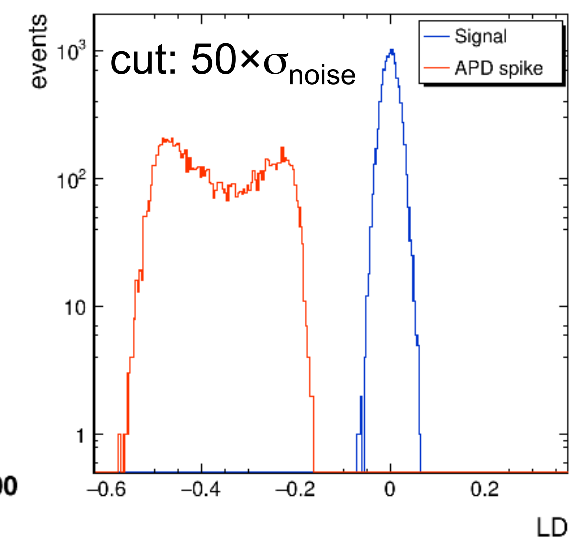
Phase-I (CMS in-situ)





TB Result

Example discriminant (TDR Simulation)



Summary

The challenging conditions foreseen at the HL-LHC require:

- ❑ Longer data pipeline, more bandwidth
- ❑ Improved spike rejection at trigger level
- ❑ Mitigation of increased APD noise
- ❑ Precision timing for vertex determination & PU mitigation

Actions to be taken in ECAL upgrade:

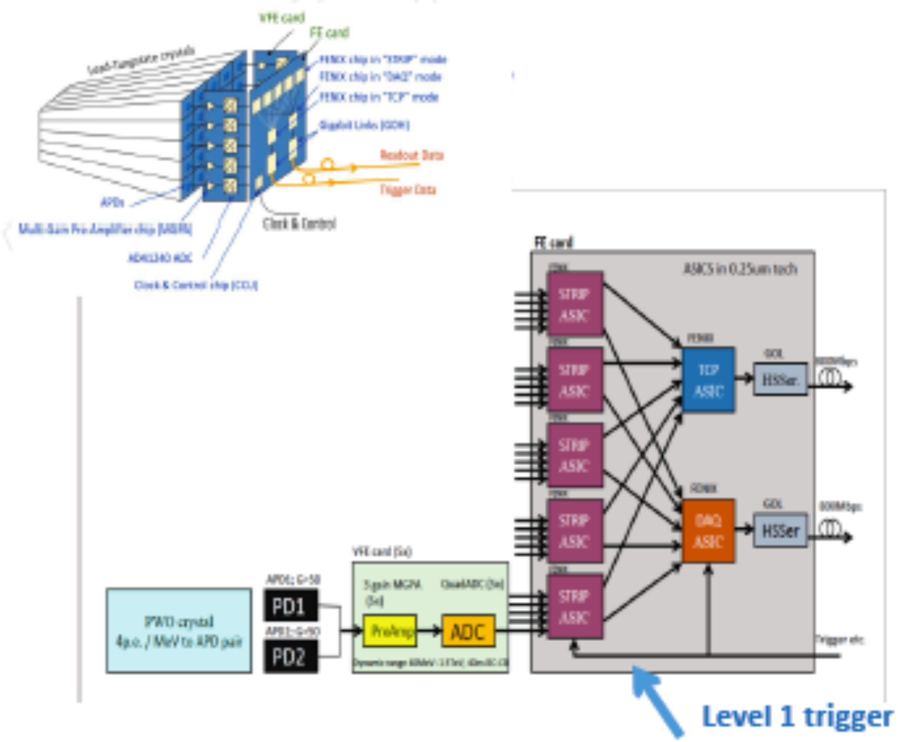
- ✓ Replace/optimize FE & VFE to cope with increased noise, PU, spikes
- ✓ Introduce precision timing
- ✓ Powerful off-detector readout cards to buffer and process higher granularity/bandwidth
  - ✓ Moving all algorithms off-detector
- ✓ Lower by 9°C the operating T to mitigate the increase of APD noise.

➡ **The ECAL upgrade will be ready to deliver high quality physics at HL-LHC**

Extra Slides

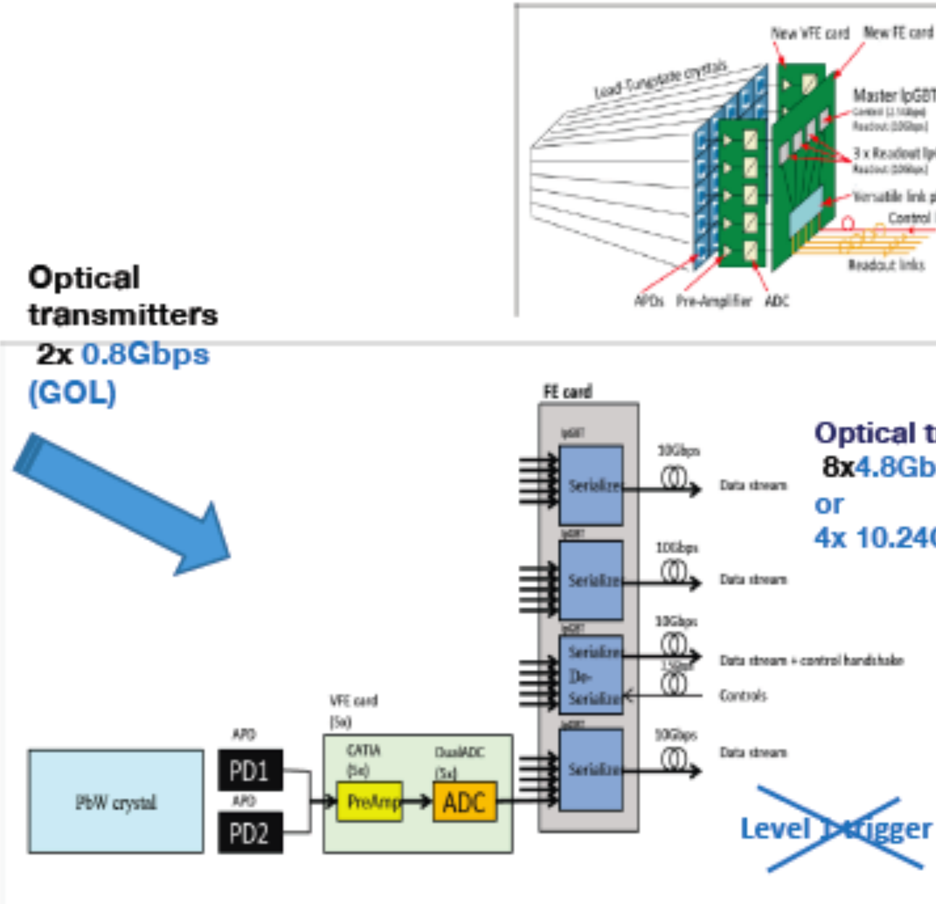
ECAL Electronics Upgrade

ECAL legacy on-detector electronics



ECAL Upgrade on-detector electronics

Optical transmitters
2x 0.8Gbps (GOL)



Optical transmitters
8x4.8Gbps (GBTx)
or
4x 10.24Gbps (lpGBT)

Data rates:

Per crystal:
- Pre-amp 3 ranges
- 12 bit ADC
- 14 bit data @ 40 MHz
- 560 Mbps data flow

Per VFE card:
- 5 crystals
- 2.8Gbps @ 40 MHz sampling

Per Trigger Tower:
- 5 VFE cards
- 14Gbps @ 40 MHz
- → 0.8Gbps TRIGGER primitives
- L1 trigger → 0.8Gbps DATA

Per VFE card:
- 5 crystals
- 10.4Gbps @ 160 MHz
- 5.4Gbps @ 160Mhz @ compression

Per Trigger Tower:
- 5 VFE cards
- 52Gbps @ 160 MHz
- 27Gbps @ 160Mhz @ compression

Crystal→APDs→VFE→FE