Status on ECL Trigger

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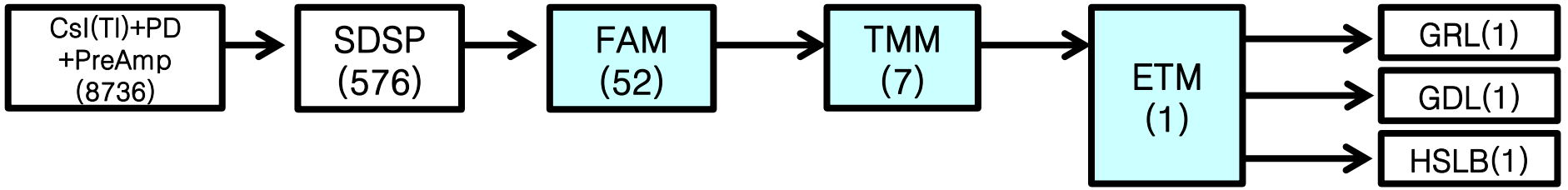
Belle II TRG/DAQ workshop @ NTU

Contents

- ECL trigger system
- ECL trigger in GCRT
- Status on b2tt and optical link
- Server ↔ modules communication method
- Slow control(detail by Cheolhun)
  - Configuration database
  - ECL trigger initialization
- Calibration
- Future upgrade
- Summary/plan

Belle2 ECL trigger system



- FAM
  - Receive 576TC analog data from ShaprDSP
    - 1TC consists of 4x4=16Xtals
  - Digitization with FADC
  - TC E&T rec. by waveform analysis(χ^2 fit) on kintex7
- TMM
  - Play an role of merger on kintex7
- ETM (report by Sunghyun)
  - ECL trigger decision by all TC E&T on virtex6
  - Send ECL trigger summary to GDL
  - Send cluster data to GRL
  - Send fired TC E&T to HSLB

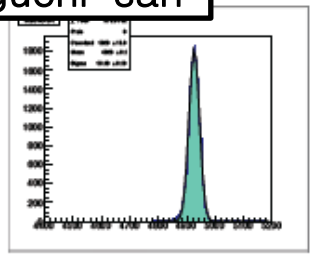
GCRT

- ECL trigger condition for GCRT
  - whenever ≥ 1TC hit with ~100MeV threshold
  - Only Barrel and backward endcap
- ECL trigger rate = ~1000Hz
- GDL trigger condition(ecl or ecl+tsfb2b(or 1tsf))
- DQM ready (report by WonJi)
- Slow control not ready (report by Cheolhun)
- Unpacker ready (report by Sunghyun)
- ECL trigger was stable during GCRT.
  - Problems found in GCRT
    - Trigger timing shift
    - Double trigger timing
    - b2link

GCRT(trigger timing shift problem)

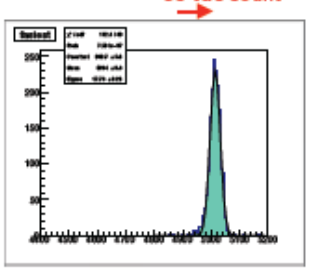
By Taniguchi-san

r2567
20170612
ECL+b2bTSF



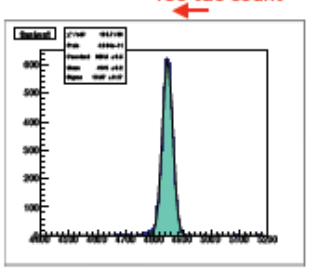
88 tdc count

r2614
20170613
ECL



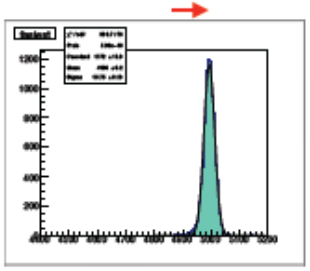
168 tdc count

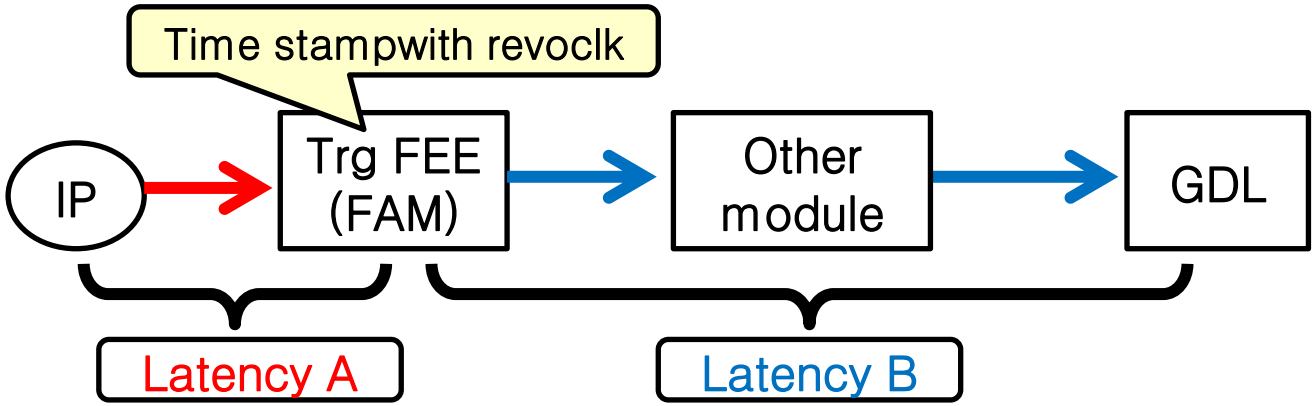
r2643
20170614
ECL



147 tdc count

r2765
20170620
ECL+singleTSF

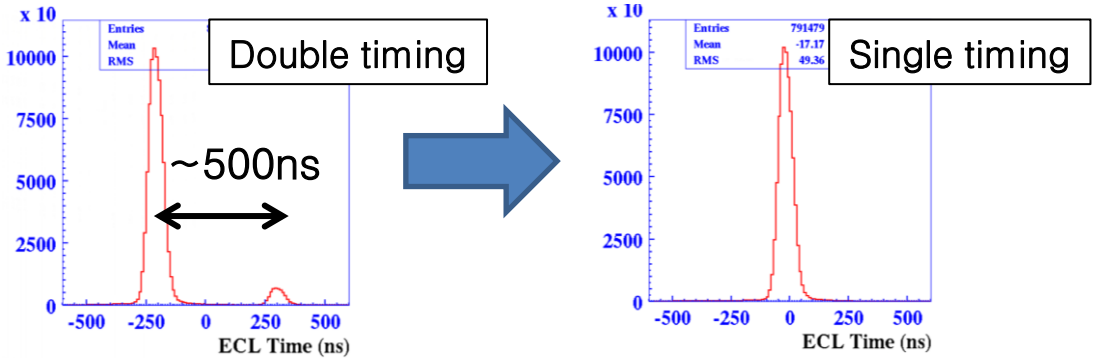




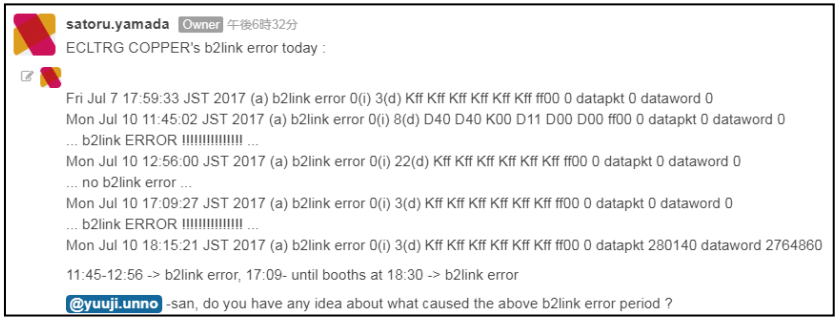
- Latency A
  - needs to be fixed by each sub trigger.
- Latency B
  - changed by firmware logic update, reboot, etc
  - change needs to be take into account in GDL
    - But it was not before, and fixed now.
- So far, latency B needs to be measured before run with some statistics, tuned by hand by nkzw-san.
- Maybe test pulse from FAM is useful for this turning for ecl trigger timing.
- Plan to check which produces T shift in ECLTRG.

GCRT(double peak and b2link problems)

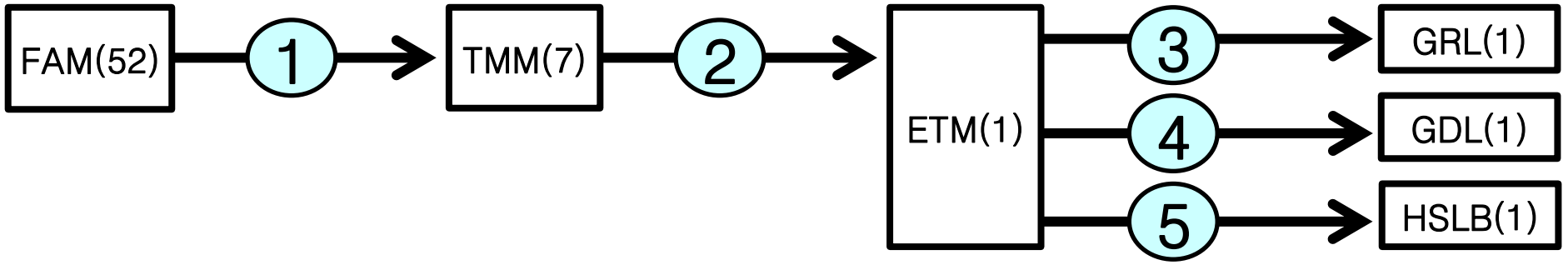
- Double trigger timing reported by Alex on 8/18
  - This appeared from run3600 (~7/20?)
  - Wrong parameters on GDL found and fixed by nkzw-san



- b2link problem at the beginning of GCR
  - So far only solution is HLSB reboot
  - Once GCRT starts, no problem
  - Probably, after
    GLOBAL→LOCAL→GLOBAL
    this problem appears(not confirmed).
  - It seems same problem exists in CDCTRG and GDL too
    - This seems to be caused by all UT3
  - investigation is not even started yet…

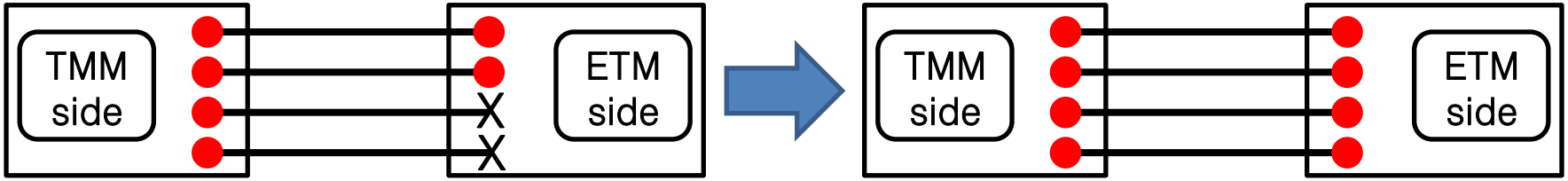


GTX/GTH link status



①All 52 GTX are very stable

②2GTX (26GTX in total by 7MPO) were unstable



- After firmware update, than very stable now.

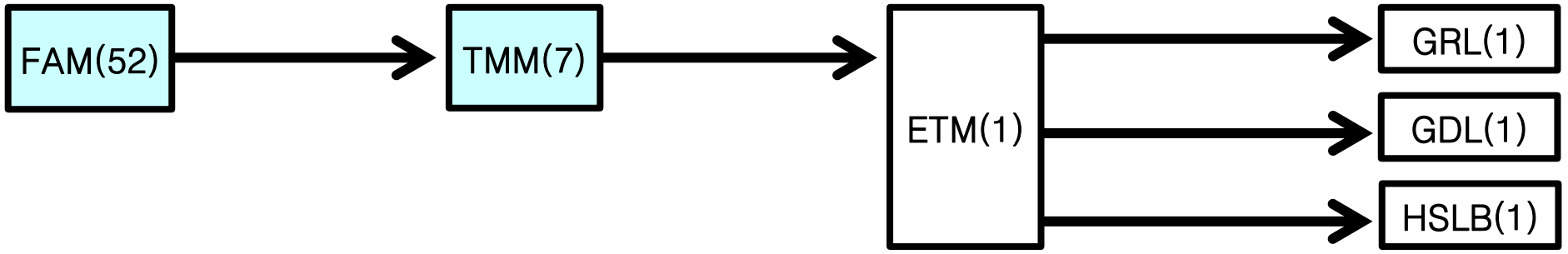
③④ 1GTX for GDL and 4 GTH for GRL were unstable

- After removing unnecessary signal in each protocol by YungTun, very stable now.

⑤Stable, but problem appears when GCR starts

- investigation after WS

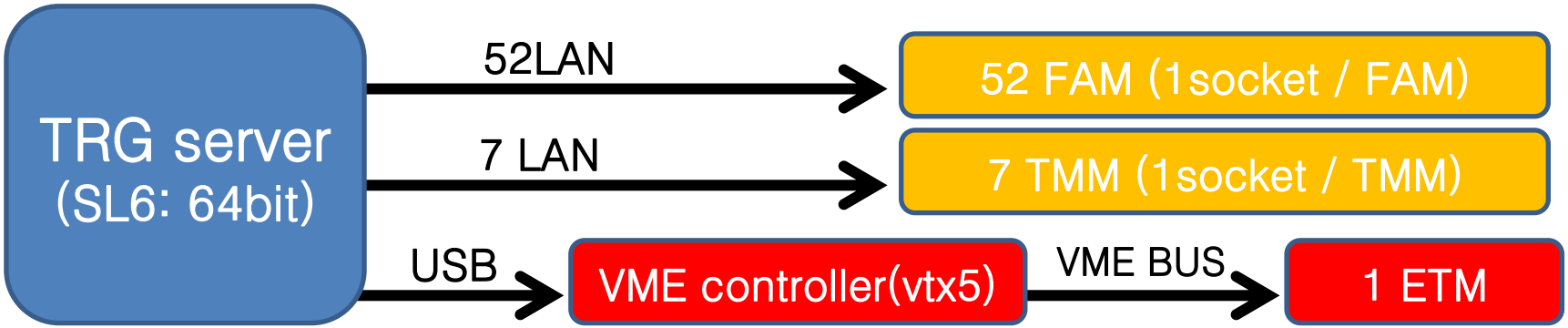
Status on b2tt down problem



- FAM
  - FAM#30 b2tt was very unstable
    - Cable replacement btw FAM#30 and FTSW solved.
  - b2tt down in all FAM during ECL stress test(high trg rate)
    - After Nakao-san updated FTSW, no problem.

- TMM
  - Just after FAM b2tt down problem disappeared, all TMM b2tt down became unstable during ECL stress test…
  - Investigation after WS.

Server ↔ modules communication



- Only single process to access to each module was available
  - FAM/TMM
    - Set W3150A+(Ethernet controller) to use 2 more sockets/FAM,TMM
  - ETM
    - Notice VME controller
      - VME power recycle needed when communication err happens
    - Replaced to VME CPU(32bit)

- Setting of boot server(SL6) for VME CPU(SL5) done.
- Start slow control setting on VME CPU(SL5) after WS.

Configuration DB parameters

Module	Par	Par decomposition	N(par)	N(bit)/par
FAM	FPGA ver	1	1	16
	CPLD ver	1	1	8
	MCU ver	1	1	8
	Module serial ID	52(FAM)	52	8
	SDSP connection	52(FAM) x 12(TC)	624	4
	Jumper for LOM	52(FAM) x 12(TC)	624	1
	T&E rec	1	1	2
	Fitter CC	52(FAM) x 12(TC) x (240+3) x 2	303264	15 (signed)
	Pedestal	52(FAM) x 12(TC)	624	12
	T offset	52(FAM) x 12(TC)	624	10
	E threshold	52(FAM) x 12(TC)	624	12
TMM	FPGA ver	1	1	16
	CPLD ver	1	1	8
	MCU ver	1	1	8
	Module serial ID	7(TMM)	7	8
	FAM connection	52(FAM)	52	8
ETM	FPGA ver	1	1	16
	Module serial ID	1(UT3)	1	8?

ECLTrg initialization

- ECL TRG initialization takes ~20 sec now
  - FAM initialization and then ETM initialization
  - Single command prepared, but not in ECLTrg SCL program
- FAM
  - Reboot (reboot + ADC data alignment) : ~5sec
  - Parameter download
    - All except for fitter CC : <1s
    - TC fitter Coefficient download : ~60sec → ~5sec

	Par decomposition	N(par)	N(bit)/par
Fitter coefficient	52(FAM) x 12(TC) x 243 x 2	303264	15 (signed)
pedestal	52(FAM) x 12(TC)	624	12 (unsigned)
E gain	52(FAM) x 12(TC)	624	12 (unsigned)
T offset	52(FAM) x 12(TC)	624	10 (unsigned)
E threshold	52(FAM) x 12(TC)	624	12 (unsigned)
T&E rec	1	1	2 (unsigned)

- ETM
  - Reboot (+ GTX reset for TMM) after FAM initialization : ~10s
    - Necessary only when GTX down and incorrect data alignment.

Calibration

(1)TC timing calibration:
- Sample: cosmic and ee/μμ/γγ, data taken by ETM B2L
- 1 or 2 / year
- ongoing with cosmic data, report by YoungJun

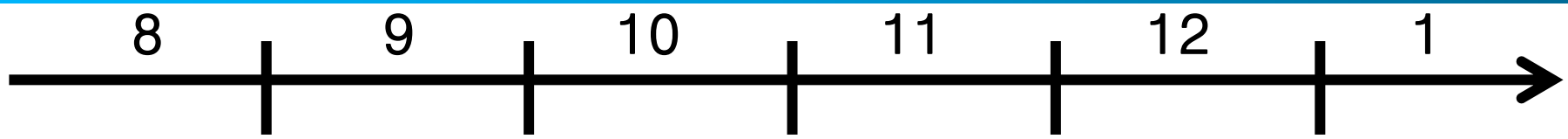
(2)TC energy calibration:
- Sample: cosmic and ee/μμ/γγ, data taken by ETM B2L
- 1 or 2 / year
- Not started yet(1st ver constant for each xtal is ready by ECL)

(3)TC energy linearity :
- Samle : test pulse from collector, data taken by FAM Ethernet
- 1 or 2 / year
- Not started yet (but, this was done @ mass production)

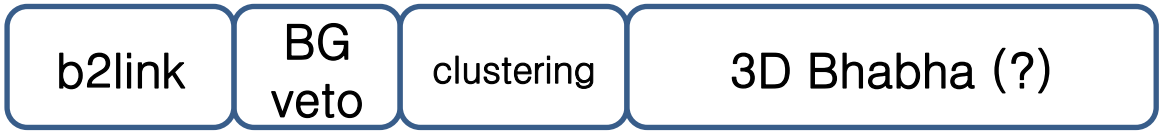
(4)TC signal shape calibration : not started
- Sample: cosmic and ee/μμ/γγ, data taken by FAM Ethernet
- 1or 2 / year
- Not started yet.

(5)Parameter of TC E&T reconstruction by χ^2 fit
- Sample: random trigger by FAM, data taken by FAM Ethernet
- Every day
- Not started yet.

Schedule

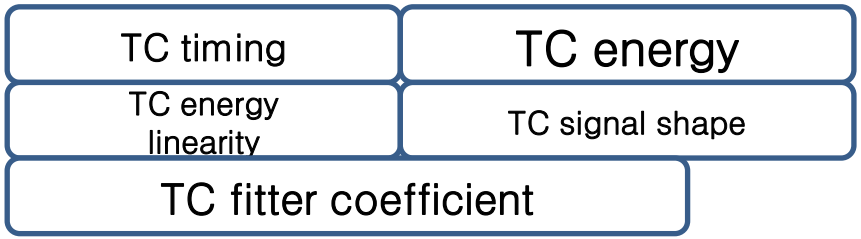


ETM FW

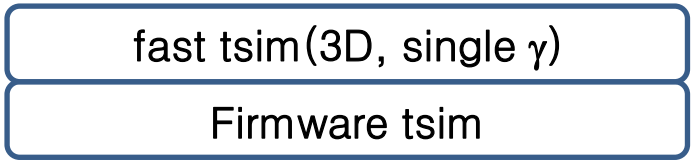


SLC

Calibration

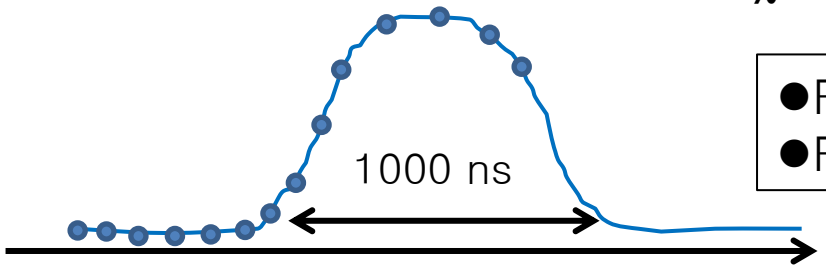


tsim



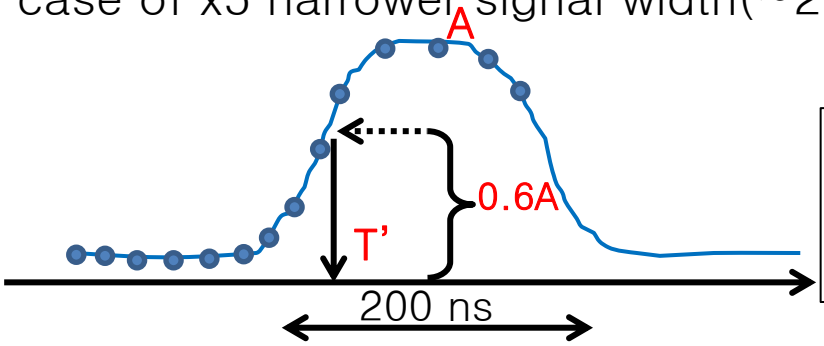
Future upgrade

- Endcap Xtal replacement to pure CsI from CsI(Tl)
  - Decay time: CsI(Tl)~1000ns → pure CsI~20ns
- In current ShaperDSP,
  - Shaping time ~ 200ns, signal width ~1000ns
- Current TC E & T reconstruction is χ^2 fit on 14 points @ every 8M data clk.



- Fit needs to finish within 125ns
- Fit is not possible for more narrower signal

- In case of x5 narrower signal width(~200ns for example)



- Measure highest point A = TC energy
- Check T' which is 0.6A
- Calculated T_0 from T' and signal shape

- FAM hardware modification is unnecessary, and only firmware modification
- Simulation study is necessary if we have any merit to chose narrower signal width and any unexpected problem or not…

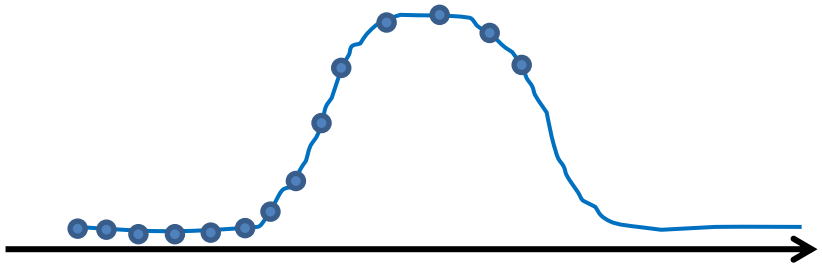
Summary / Plan

- ECL trigger is stable in GCRT
- Investigation of TMM b2tt, ETM b2link after WS
- Start using VME cpu for ETM
  - ECL trg SCL would be ready in a few months
- Many things to be done remain for phase2
  - All will be done in this year

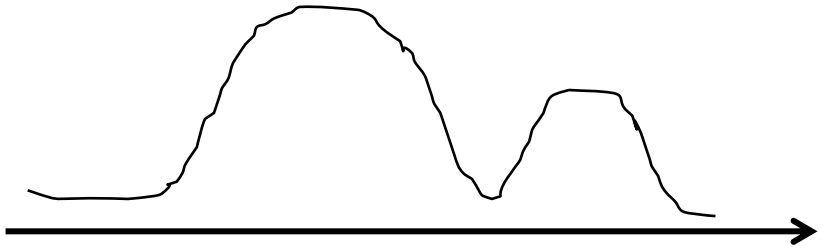
backup

Future upgrade

- Current TC E & T reconstruction is χ^2 fit on 14 points @ every 8M data clk.



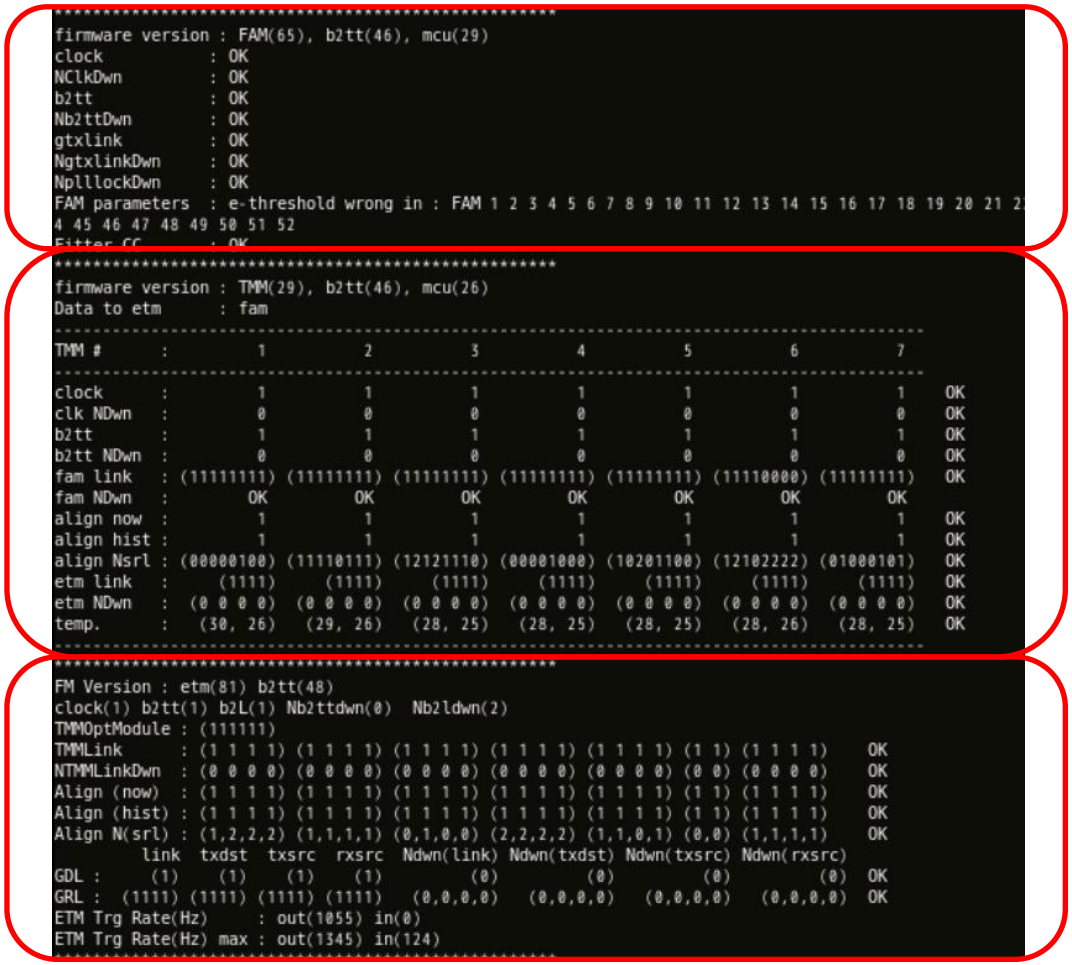
- If TC hit is detected, next fit result is not sent to TMM in ~2μs
  - assuming no signal come in next ~2μs
  - if two signal are too near, fitter doesn't work.
- In case of two signal in short time (peak position difference > 500 ns)



  - Fit 1st peak
  - Subtract data point based on fit on 1st peak
  - Fit 2nd peak

  - Tsim study by InSoo, if peak position difference is < 500ns, fitter works.
  - No significant efficiency gain for BB+beambkg was found (a few years ago)
  - It would worth to check this again with recent beambkg sample too(?)
  - Probably all calculation within 125ns on firmware is possible.

Condition of “ECLTRG Ready”



```
************************************************
firmware version : FAM(65), b2tt(46), mcu(29)
clock           : OK
NClkDwn         : OK
b2tt            : OK
Nb2ttDwn        : OK
gtxlink         : OK
NgtxlinkDwn     : OK
NplllockDwn     : OK
FAM parameters  : e-threshold wrong in : FAM 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 2
4 45 46 47 48 49 50 51 52
Fitter CC       : OK
```

FAM

```
************************************************
firmware version : TMM(29), b2tt(46), mcu(26)
Data to etm      : fam
-------------------------------------------------------------------------------------------
TMM #      :         1          2          3          4          5          6          7
-------------------------------------------------------------------------------------------
clock      :         1          1          1          1          1          1          1    OK
clk NDwn   :         0          0          0          0          0          0          0    OK
b2tt       :         1          1          1          1          1          1          1    OK
b2tt NDwn  :         0          0          0          0          0          0          0    OK
fam link   : (11111111) (11111111) (11111111) (11111111) (11111111) (11110000) (11111111)   OK
fam NDwn   :        OK         OK         OK         OK         OK         OK         OK
align now  :         1          1          1          1          1          1          1    OK
align hist :         1          1          1          1          1          1          1    OK
align Nsrl : (00000100) (11110111) (12121110) (00001000) (10201100) (12102222) (01000101)   OK
etm link   :     (1111)     (1111)     (1111)     (1111)     (1111)     (1111)     (1111)   OK
etm NDwn   :  (0 0 0 0)  (0 0 0 0)  (0 0 0 0)  (0 0 0 0)  (0 0 0 0)  (0 0 0 0)  (0 0 0 0)   OK
temp.      :   (30, 26)   (29, 26)   (28, 25)   (28, 25)   (28, 25)   (28, 26)   (28, 25)   OK
-------------------------------------------------------------------------------------------
```

TMM

```
************************************************
FM Version : etm(81) b2tt(48)
clock(1) b2tt(1) b2L(1) Nb2ttdwn(0)  Nb2ldwn(2)
TMMOptModule : (111111)
TMMLink      : (1 1 1 1) (1 1 1 1) (1 1 1 1) (1 1 1 1) (1 1) (1 1 1 1)    OK
NTMMLinkDwn  : (0 0 0 0) (0 0 0 0) (0 0 0 0) (0 0 0 0) (0 0) (0 0 0 0)    OK
Align (now)  : (1 1 1 1) (1 1 1 1) (1 1 1 1) (1 1 1 1) (1 1) (1 1 1 1)    OK
Align (hist) : (1 1 1 1) (1 1 1 1) (1 1 1 1) (1 1 1 1) (1 1) (1 1 1 1)    OK
Align N(srl) : (1,2,2,2) (1,1,1,1) (0,1,0,0) (2,2,2,2) (1,1,0,1) (0,0) (1,1,1,1)    OK
          link  txdst  txsrc  rxsrc  Ndwn(link) Ndwn(txdst) Ndwn(txsrc) Ndwn(rxsrc)
GDL :      (1)    (1)    (1)    (1)         (0)         (0)         (0)         (0)  OK
GRL :  (1111) (1111) (1111) (1111)   (0,0,0,0)   (0,0,0,0)   (0,0,0,0)   (0,0,0,0)  OK
ETM Trg Rate(Hz)     : out(1055) in(0)
ETM Trg Rate(Hz) max : out(1345) in(124)
************************************************
```

ETM

- Currently, check each outputs from monitoring system.
- Should prepare single flag to know all ready or not.

Condition of “ECLTRG Ready”

- FAM
  - Firmware(FPGA, MCU) ok
  - Parameter download ok
  - Clock and b2tt up
  - GTX link up
  - ADC data alignment ok (check pedestal(!?))
- TMM
  - Firmware(FPGA,MCU) ok
  - Clock and b2tt up
  - GTX link up (both FAM and ETM)
  - FAM data alignment ok
- ETM
  - Firmware(FPGA) ok
  - Clock and b2tt up
  - GTX/GRL link up(all TMM, GDL, GRL)
  - TMM data alignment ok

Download par → extraction par from all boards → compare par with DB

Attenuator setting on ShaperDSP

Single crystal energy calibration
ECLDigit → ECLCalDigit

- Energy (GeV) = Amplitude (ADC counts) × C_e × C_s
- C_e = electronics calibration (1 in this study)
- C_s = single crystal energy calibration

- Energy constant (BR+BE) prepared
- Two gain setting on ShaperDSP
  - 6 bit(0–63, LSB~1%gain) parameter
    - Original setting is 3F(111111)
  - Jumper on/off
    - "on" give x2 gain

- Check w/ and w/o energy constant on ShaperDSP
  - But, no change observed in ecl trigger rate…
  - → found 6 bit parameters were not set correctly
  - → we will try again later
- Alex found non-linearity of 6 bit attenuator setting
  - →need correction for this too…

FAM parameter check

	Par decomposition	N(par)	N(bit)/par
Fitter CC	52(FAM) x 12(TC) x 243 x 2	303264	15 (signed)
pedestal	52(FAM) x 12(TC)	624	12 (unsigned)
E gain	52(FAM) x 12(TC)	624	12 (unsigned)
T offset	52(FAM) x 12(TC)	624	10 (unsigned)
E threshold	52(FAM) x 12(TC)	624	12 (unsigned)
T&E rec	1	1	2 (unsigned)

- Download par → extraction par → compare par with DB
- All parameters can be extracted from FPGA through TRG server easily and quickly(<1s) except for inputted pedestal value.
- In pedestal case, we can obtain measured value from FPGA quickly and check if |ped−500|<5 or not.
- For fitter CC, there are 3 values for each set of 52(FAM)x12(TC) which show CC version. By checking the 3 numbers, parameter confirmation can be easily and quickly done.

Prospect for phase 2 (my personal concern)

- More tsim studies are necessary
  - Beambkg > expectation case
    - Higher TC E threshold !?
    - Exclude forward endcap !?
    - Effect needs to be checked
  - Single γ
    - Trg rate with beambkg is not estimated yet
    - CDC trg timing in tsim ?
  - Lower TC energy threshold !?
  - 3D Bhabha
    - Enough gain can be obtained !?

Background level	Physics trigger rate(KHz)
x 1	1.5 ±0.14
x 2	8.0 ±0.75
X 5	89.2 ±1.20

SINGLE PHOTON TRIGGERS

	γγ	Bhabha		Total
1 GeV*	0.2 nb	0.4 nb	1.6 nb	2.2 nb
2 GeV*	0.5 nb	2.9 nb	0.1 nb	3.5 nb

- The efficiency of the ECL trigger for muon pairs could be improved with a slightly lower ECL threshold.
- Two-photon production of π^0 and low-mass ALP requires lower ECL thresholds.

- ETM firmware development
  - Development of each necessary logic would be ok
    - 2D Bhahba, ICN, b2link readout, beambkg veto, clustering…
    - 3D bhabha might need some time…
  - Not sure ETM works correctly when all logic are combined…