Past experience and present R&D at LAL/SERDI (Electronique, Research on Detectors and Instrumentation Department) in view of a participation to BELLE II upgrade

Belle II Trigger/DAQ workshop, Taipei, August 25th 2017

Dominique Breton, Jihane Maalmi

LAL (Linear Accelerator Laboratory), Orsay - France

CNRS - LAL : Research Lab on particle physics, cosmology and astrophysics
135 researchers, 174 engineers and technicians

*(located in the Scientific Campus of **Orsay, Paris-Saclay University**)*

LAL Structure

- Security
- Communication
- **Director: Achille Stocchi**
  Deputy: **F. Cavalier**
- Scientific Council
- Lab Council
- Interface with Industry

- Physics Groups
- Accelerator Department
- SADM (Administration)
- SDTM (Mechanics)
- SERDI (Detector & Electronics) D. Breton
- SI (Computer Science)
- SPPI (Infrastructure)

SERDI department

Department created in January 2012 based on both Electronics (S.E) and Research on Detectors (GRED) groups, whose role is to:

- Build apparatus for **physics programs** but also for **specific R&D programs** **in electronics and detectors**
- Face the challenges of the **big international projects**
- Build small and medium **caracterization platforms** for detectors and their associated electronics
- Respond to the rising amount of **local projects** (P2IO, Equipex, …)
- Maintain and improve our **technical expertise** (new ambitious projects, collaborations with other laboratories, R&D, teaching, …)
- **Promote our develoments for industrial applications** with all the necessary precautions (intellectual protection, patents, licenses, contracts with well mastered commitment)

SERDI
Service d'Electronique, Recherche en Détecteurs et Instrumentation

April 2017

42 persons

Head: **Dominique Breton** (IPP1)
Deputy: Véronique Puill (IR1)

Secretary: Vanessa Bénard (TCN)

Driving comity:
Head of department
Head of groups

Instrumentation

F. Wicek (IR1)
Head

C. Cheikali (IE2)
R. Chiche (IR1)
P. Cornebise (AI)
M. Gaspard (IEHC)
J. Jéglot (IE2)
D. Jehanno (AI)
J. Girault (TCN)
S. Trochet # (TCE)
C. Sylvia (AI)

Systems

C. Beigbeder (IR1)
Head

T. Cacérès (IEHC)
D. Charlet (IR2)
B.Y Ky (ASI)
J. Maalmi (IR2)
E. Plaige (IE1)
S. Simion (IR1)
V. Truong Canh
(Apprenti)

Research on Detectors

V. Puill (IR1)
Head

P. Barrillon (IR1)
L. Burmistrov (IR2)
S. Dubos (IR)
V. Chaumat (AI)
P. Halin (TCS)
P. Loaiza (IR2)
A. Natochii
(Doctorant)

Microelectronics

P. Vallerand (IR1)
Head

M. Cohen Solal (IR2)
M. El Berni Δ (IE2)
O. Lemaire (IR2)

CAD/Fabrication

O. Duarte (IR1)
Head

CAD

P. Rusquart ◊ (AI)
C. De Andrade (AI)
J-Ch. Hernandez (TCN)
C. Mendy (TCN)
J-L Socha (TCS)

Fabrication

P. Favre (TCE)
F. Campos (TCN)
B. Debennerot (TCS)
M. Fernandez (TCS)

 # support machine CMS
Responsable plateforme Captinnov

Δ support outils VLSI

◊ support outils CAO PCB

Past projects at SERDI

Still running or recently terminated

CERN

ATLAS (Lar calo, Alpha)

LHCb (calo)

Neutrinos

Nemo III

Cosmology/Astroparticles

VIRGO

BAO

Planck

LSST

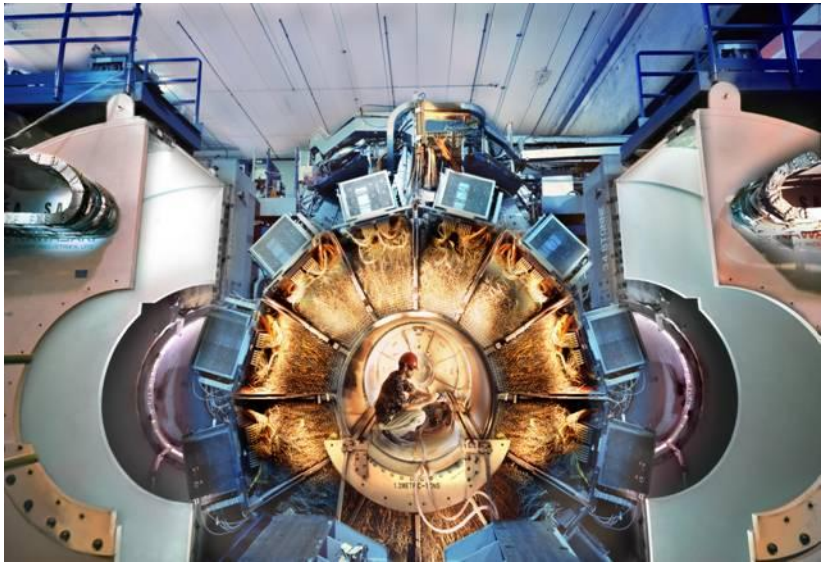
EP colliders

BABAR (SLAC)

SuperB (Roma)

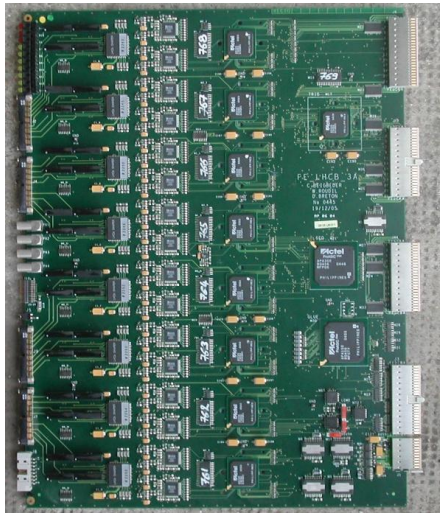
Focus on projects implying TDAQ

- **BABAR**: Front-End & Readout Electronics for DIRC subdetector
  - 12 crates / 10,752 channels
  - Fully controlled and readout by Gbit optical fibers

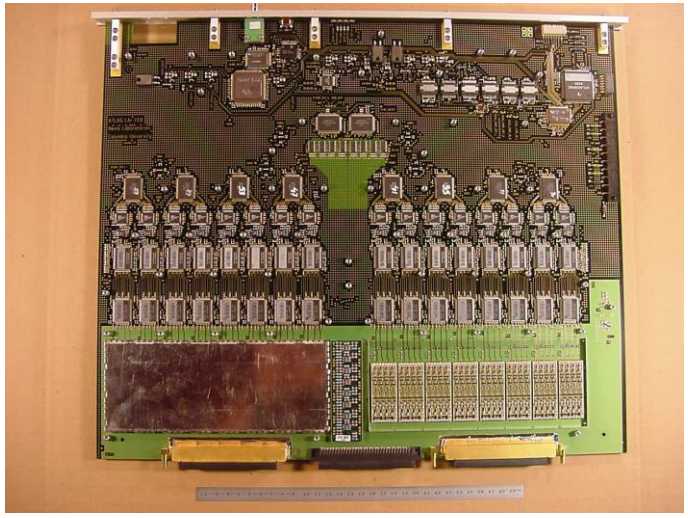


- **ATLAS**: Front-End board for the LARG Calorimeter
  - 1628 boards produced and fully characterized
  - 200,000 channels @ 300krads of radiation

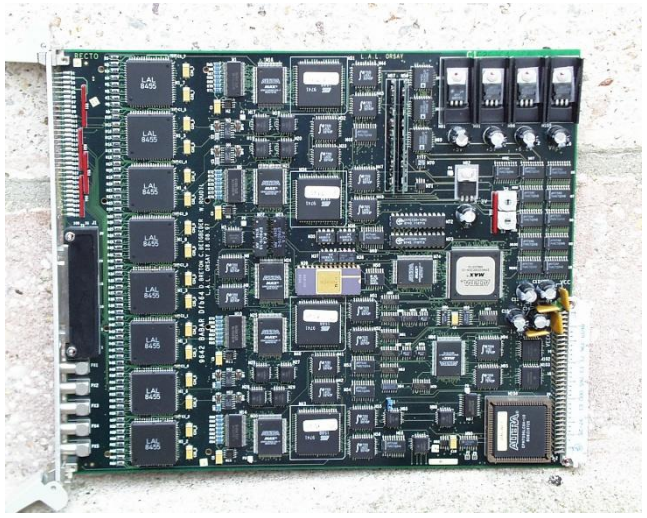
- **LHCb**: Front-End and Trigger Electronics for Calorimeters
  - 28 crates / 7,500 channels
  - Smart L0 trigger, interconnecting the 28 crates via ~1000 CAT6+ cables (bidirectionnal serial links)



LHCb calo FE board



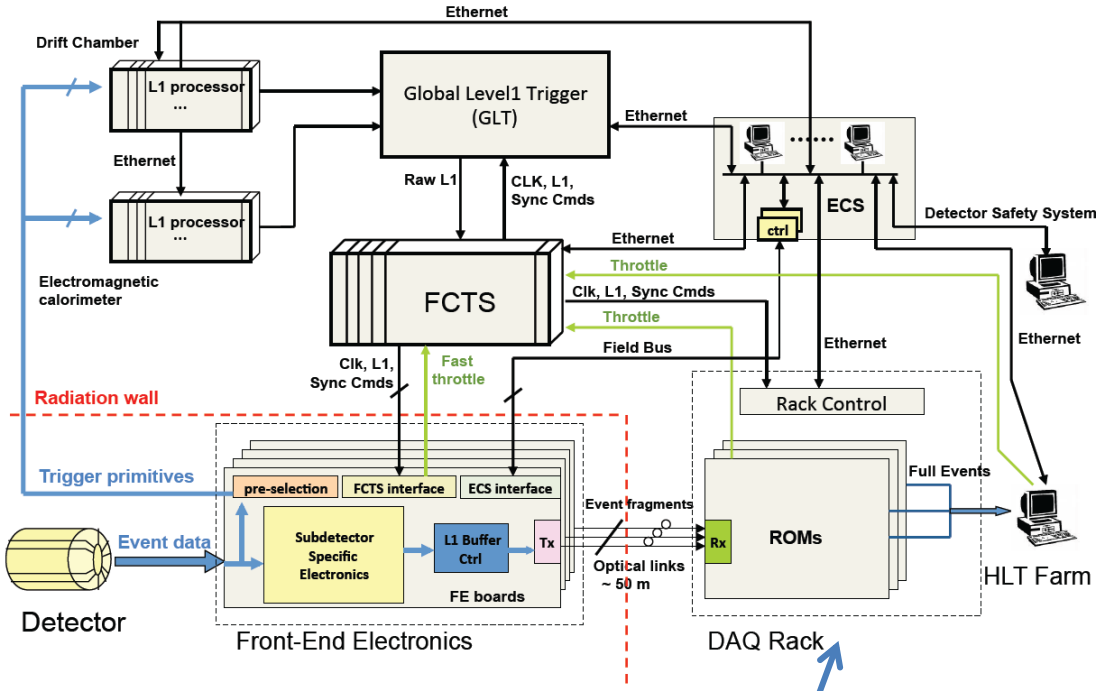
ATLAS LARG calo FE board

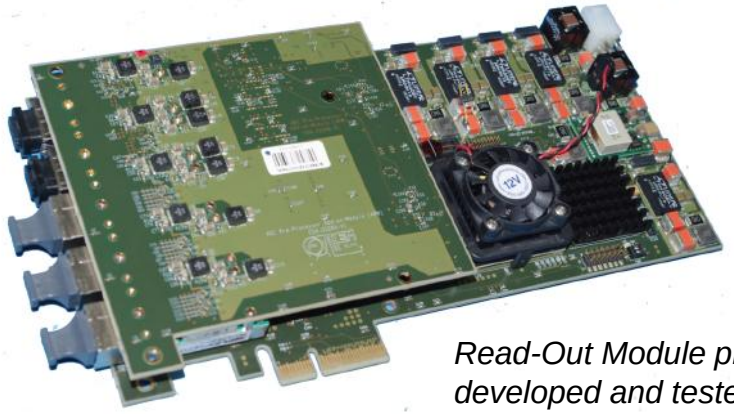


BABAR DIRC FE board

SuperB

- We were deeply involved in the **SuperB** project
- We were major actors of the **definition of the detailed architecture** of the full system including:
  - FCTS (Fast Control and Timing System)
  - Common Readout System and DAQ
  - First Level Trigger
  - ECS (Electronics Control System)
- Dominique Breton was the **Electronics Coordinator** of the project
- The project was stopped right after the **TDR** was published …
- Many developed solutions had a second life, like the PCIe acquisition board which drove to PCIe40 for LHCb upgrade





Read-Out Module prototype developed and tested For SuperB

Current projects at SERDI

CERN

ATLAS (Pixels, Lar calo)

LHCb (calo)

Neutrinos

SuperNemo

Intense Xray Source

ThomX

Cosmology/Astroparticles

VIRGO

BAO/PAON

EUSO

LSST

EP colliders

ILC (CALICE)

SuperKEK-b (beam)

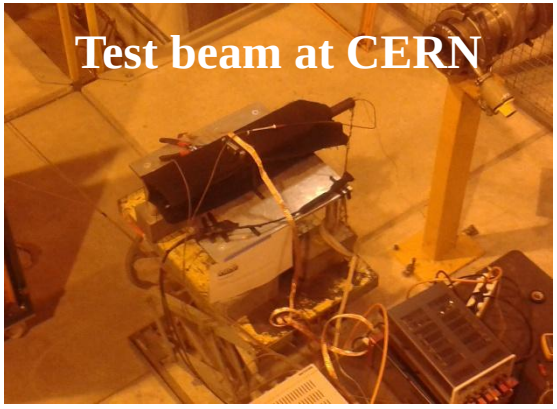
Belle II

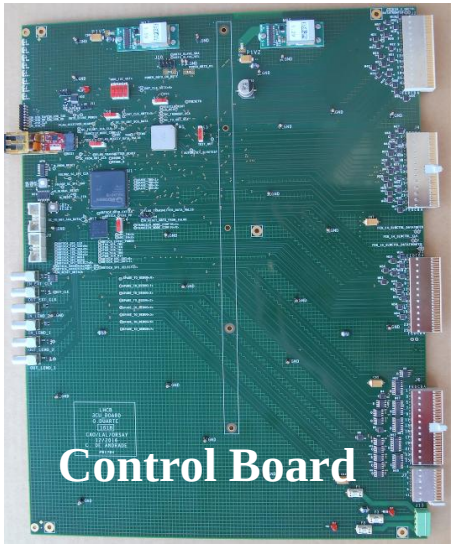
Own projets

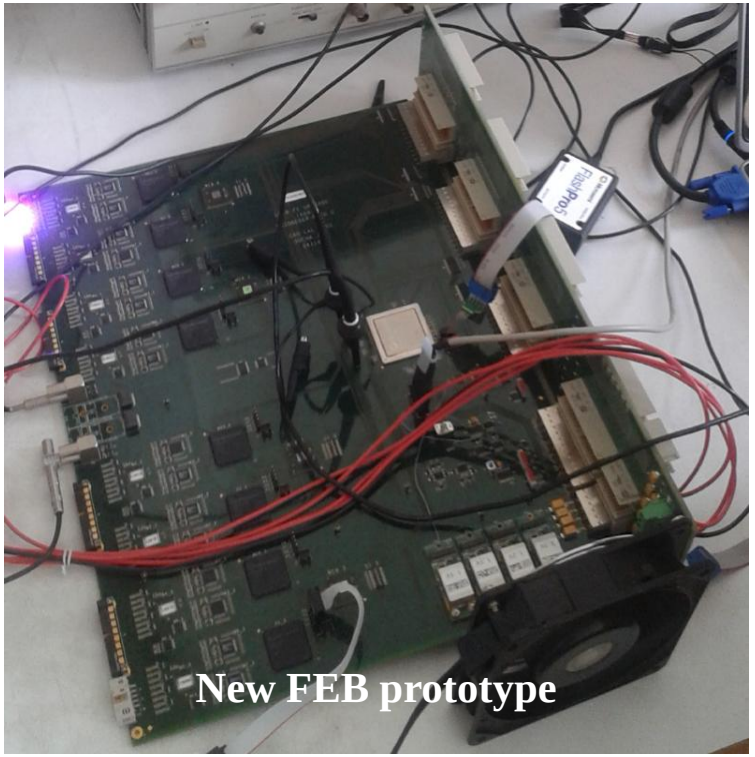
(other slide)

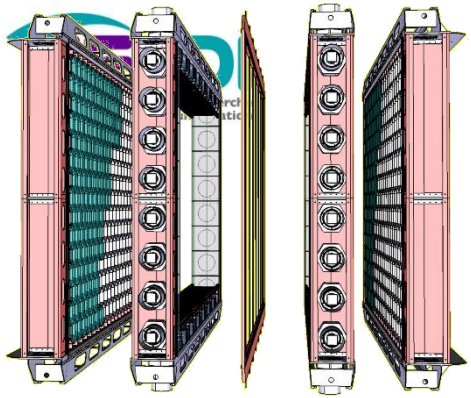
LHCb

- Upgrade of the calorimeter FE electronics => **triggerless DAQ**
- Full speed digitization of signal => 40 MHz * 12 bits / channel
- 4 GBTs (CERN new rad-hard serializers) + fibers / FE board => 10 Gbits/s
- Need to design and produce new versions:
  - ~300 FEB ECAL + HCAL
  - ~30 Control boards
- Status :
  - Finalizing the design.
  - Teams beams and radiation tests.
- Project in collaboration with
  - Barcelone, Valence → ASIC
  - CERN, ITEP, IHEP, INR → HV, Monitoring, calibration
  - LAPP → DAQ
  - LLR → “control command” software (LHCb Lab.)
  - LPC → dismantling of SPD/PS









SuperNemo

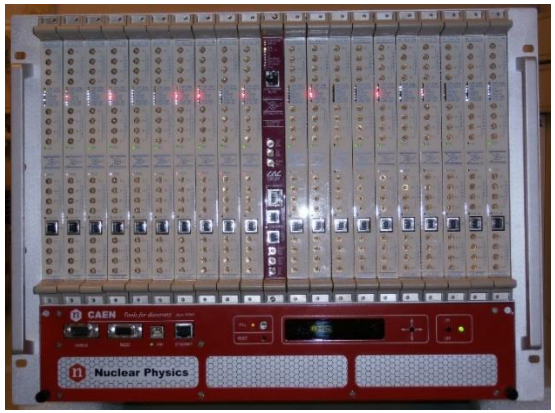
Research of the direct observation of a 2β0ν double beta desintegration in Modane

- **Prototype Module: Tracker (drift chamber) (6,102 Ch) + Calorimeter (712 Ch)**
- **LAL is in charge of the whole electronics system (DAQ and Software libraries included) except the Tracker Front-End Board hardware**
- **Based on the home-made secured Gbit UDP and custom backplanes developped at LAL (high speed links, Clock, Trigger, FPGA firmware reconfig)**
- **6 (+1 spare) Front End Electronics Crates (Tracker and Calorimeter)**

56 Calorimeter Front End Boards, based on the SAMLONG Asics (*used here @ 2,56 GS/s*) *12 Bits Analog Memories*

6 (+ 4 spare) Control Boards (cabled @ LAL): Clock Distribution and high speed links for the Control/Readout of the FE boards.

1 (+ 1 spare) Trigger Board (cabled @ LAL): System Clock Distribution toward Control Boards + Trigger decisions (Calo and Tracker)



Custom backplane

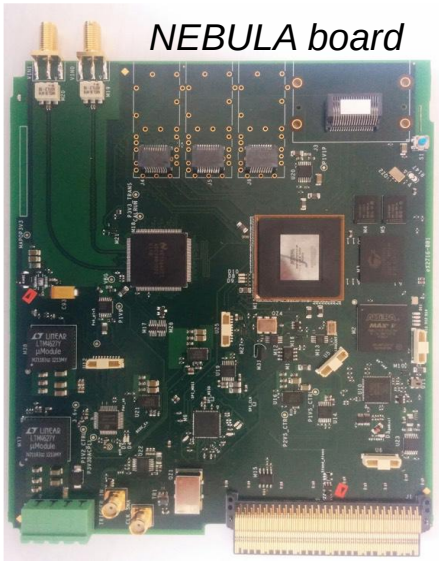
BAO/PAON/NEBULA/DAQGEN

BAO radio : radio-astronomy experiment based on the study of the 21 cm ray of extra-galactic hydrogen

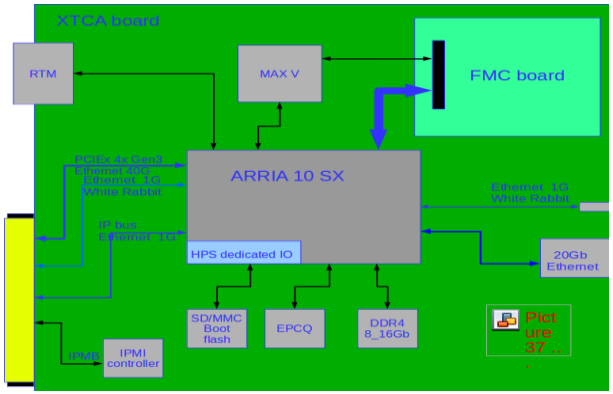
PAON-4 is a prototype with 4 antennas installed at the Nançay observatory and whose electronics has been developed at LAL for BAO

- The **NEBULA** board is a prototype for a new digitizer located at the foot of the antenna (2 channels, 1GS/s), interfaced via 10 Gbits/s Ethernet optical fibers and using White Rabbit.
- **DAQGEN** is an IN2P3 multi-lab **R&D** project aiming at realizing an acquisition system based on xTCA.4. LAL is in charge of the project coordination and of the HALOGEN board.
- **HALOGEN** : xTCA motherboard based on ARRIA 10 and using White Rabbit, slots for FMC, 40 Gbits/s PCI-e backplane connection, 20 Gbits/s Ethernet optical link on front panel, aimed at replacing the NEBULA board once equipped with a 2-channel ADC FMC board.

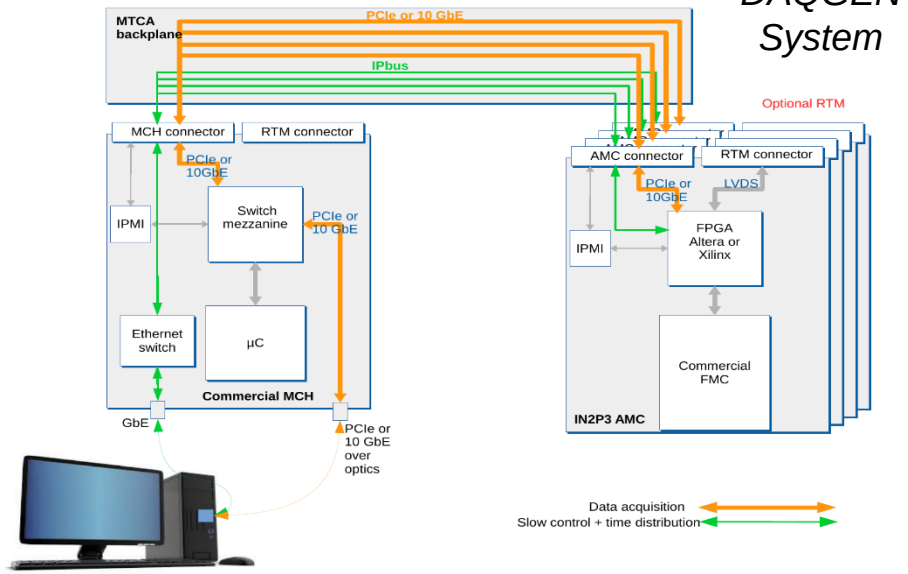
NEBULA board



HALOGEN board



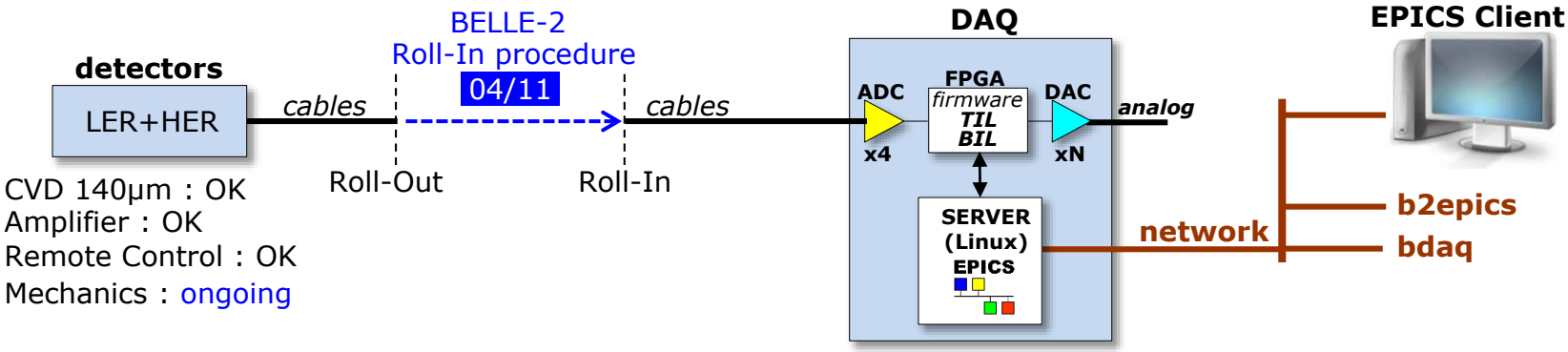
DAQGEN System



SuperKEK-b

Design of the deadtime-less acquisition system
of the **luminosity detector built at LAL** and based on diamond detectors

Template GUI for EPICS Client with CSS BOY : to be developped



CVD 140µm : OK
Amplifier : OK
Remote Control : OK
Mechanics : ongoing

DAQ rack: ongoing
ADC 1GSPS : OK
FPGA : firmware OK, under test
DAC : TBD
Server : ongoing
EPICS : to be integrated

Estimated end of development :
end of 2017

Network is used to :
SEND Luminosity EPICS PVs (TIL, BIL,…)
RECEIVE SuperKEKB/BELLE2 PV (Current, Pressure, Fill Pattern, …)

SERDI's current own projects

Medical imaging
SiPMED/SONIM
(with *IMNC*)

R&D on detection systems & µE
Beam: UA9 => CERN, SPS & LHC
Front End: Cherenkov Lab

Transversal Projects

LAL-Usb
LAL-Udp

R&D Electronics & µE
WaveCatchers
SAMPIC
RD53 (ATLAS)

Platforms
CaptInnov
CORTO

Standard interface developments
(USB & UDP)

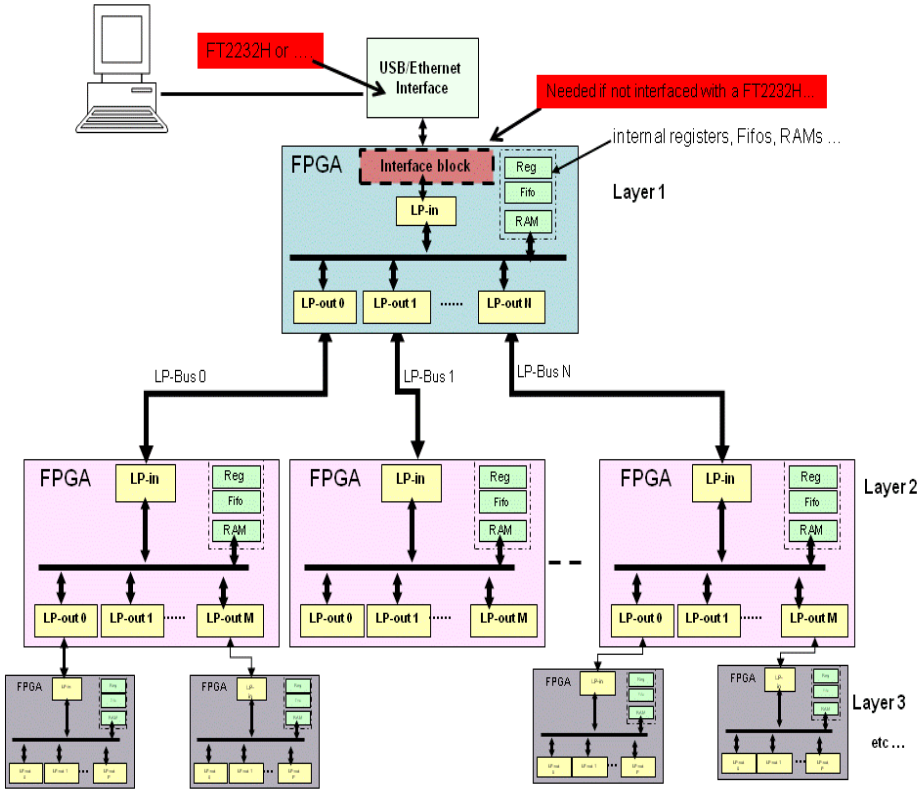
Aim of the R&D: to propose a **simple and cheap plug&play solution** for the use of **USB** and **UDP** in the boards and systems. The protocol has been developed at LAL. The solution includes ***commercial hardware, custom firmware blocks and software librairies***, plus the possibility to **reprogram the FPGAs**.

Schedule of the project: continuous since 2007.

1) **Standard USB interface**: for all the applications where there is a single FPGA on the board, or where event data acquisition is not managed by USB.

2) **Multi-layer USB interface**: for multi-channel applications where event data acquisition is managed by USB and has to be optimized. Based on a « russian doll » data encapsulation philosophy and on a data-push readout. Especially adapted for tree-like systems or systems with sparsified readout.

3) **Multi-layer Gbit UDP interface**: same as multi-layer USB with a top level UDP interface to computer. No need of FGPA with fast serializers or external RAM => cheap solution. **Data stream is secured: no data loss (TCP like but without deadtime)!**



Project status: fully operational.

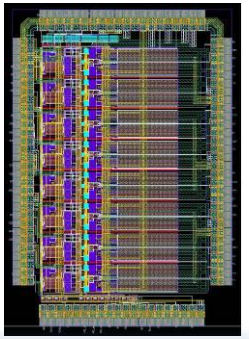
Users: most of the projects and test benches at LAL. Also **used by many other labs**.

Activities in µ-electronics

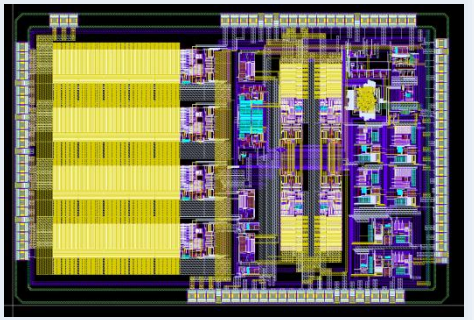
- LSST (LAL-LPNHE collaboration): over (AMS CMOS 0.35µm 5V & HV)
  - ASPIC (Analog Signal Processing asIC): FE chip for CCD
  - CABAC (Clock And Bias Asic for CCD): clock and polarization controller chip for CCD

  → production & test of 1500 ASPIC + 100 CABAC

• **ASPIC IV** : 2,7x3,8 mm²
• AMS CMOS 0.35µm 5V



• **CABAC1**: 9x6 mm²
• AMS CMOS 0.35µm HV



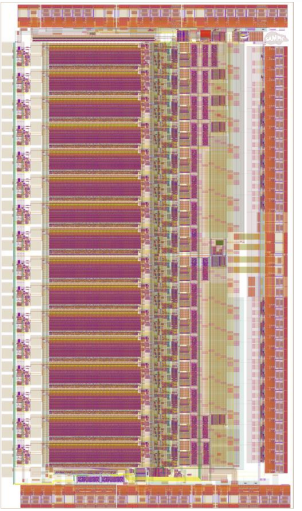
- Picosecond Timing (LAL-IRFU collaboration): ongoing
  - SAMPIC (SAMpler for PICosecond time pick-off) (AMS CMOS 180nm)

  → SAMPIC_V3 will arrive end of Sept 2017

- RD53 – SLHC (TSMC-IMEC 65nm) : new
  - Test chip C3 for pixels => 100% operational

  → block for radiation dose monitoring delivered to CERN

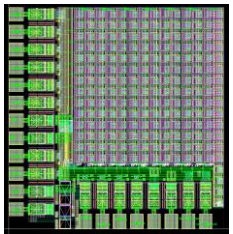
• SAMPIC3: 1,95x3,66 mm²
• AMS CMOS 180nm 1.8V



- R&D Cherenkov Lab (LAL-LPC Caen collaboration): new (AMS CMOS 180nm)
  - Front-End Chip + TDC for SiPM, PMT & MCP-PMT

  → prototype chip submission in 2017

- R&D UA9: double charge integration chip for SPS & LHC: new (AMS CMOS 0.35µm)
  - for real-time proton counting with a high flexibility



R&D on Waveform Digitizers

R&D systems

• The **WaveCatcher family** proposes a cheap but effective plug & play solution for capturing fast signals and performing real-time measurements.
  - All the boards are based on the **SAMLONG** analog memory, developed commonly with Irfu.
  - Equipped with **home-made USB & UDP interfaces**.

• Many different versions have been developed:
  - 2-channel USB-powered
  - 8-channel desktop
  - 16-channel desktop
  - 64+8-channel mini crate

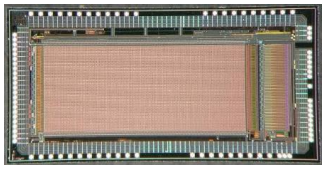
The WaveCatcher Logo

• The performances of these boards are a reference in the domain: **3.2GS/s, 12 bits, 500 MHz bandwidth, 2.5V dynamic range, 0.7mV rms noise, time precision < 5 ps rms, smart trigger.**

• A powerful **control and acquisition software** has been developed with its libraries (Windows and Linux). It offers a system **equivalent to up to a 64+8-channel oscilloscope**.

• **Used worldwide by many projects, univ., labs and companies** (BiPo, SUPERNEMO, Codalema, CORTO, UA9, IRFU, CERN, INFN, PSI, BNL, Rochester, SLAC, Osaka, Barcelona, Dublin, LPSC, IPNO, IPHC, APC, CENBG, IMNC, Subatech, Nançay, Ganil, Cadarache, SENSL, GE, Hamamatsu, Solayl, PHIL, Eli_NP, LSM, SHIP, Frascati, …) => **user Workshop (with SAMPIC) at LAL early 2018 (Jihane)**

• **Both hardware and software have been valorized and are sold under license by CAEN (X743 family) and M2J.**

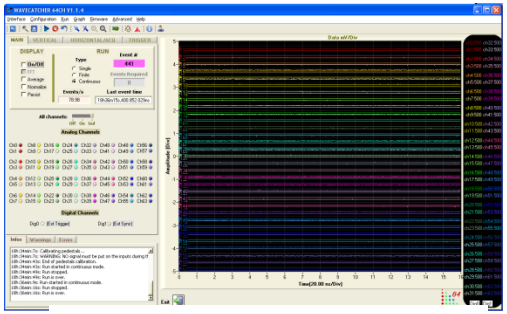


SAMLONG ASIC

WAVECAT_16CH

64-channel WAVECATCHER crate

CAEN modules



64-channel WAVECATCHER software

SAMPIC: the ps Waveform TDC

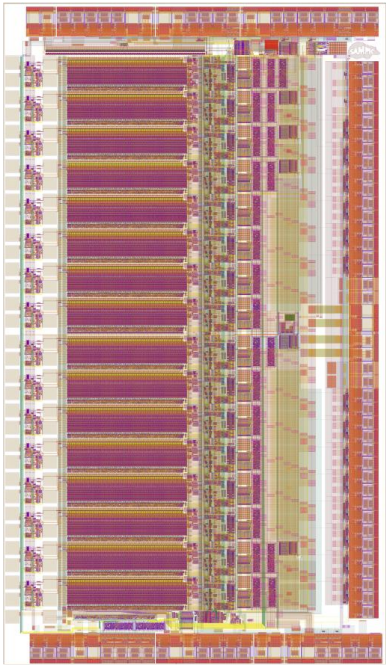
➢ Waveform TDC: works on **analog** signals !

The SAMPIC Logo on silicon !

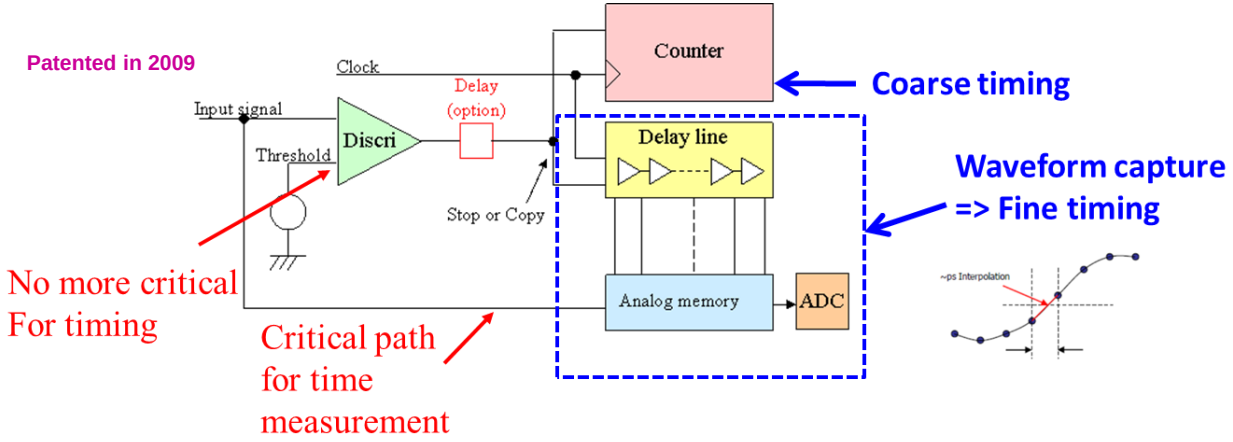
- Technology: AMS CMOS 180nm
- The chip houses **16 channels each with 64 analog memory cells**
  - ⇒ Sampling up to **10.24 GS/s** (standard main clock is **160 MHz**)
  - ⇒ Signal bandwidth is **>> 1 GHz**
- Internal massively parallel 8/11-bit Wilkinson ADC running at **1.3 GHz** in each cell => short conversion time
- **The chip is a complete system (smart trigger, tunable ADC, fast readout …)**
- **A 32-channel acquisition module** has been designed together with its **dedicated software and library (already widely used at CERN)**.
  - 256 channel system is being designed
- **Measured time precision: < 3 ps rms !**

  => many modules already used worldwide (CERN, US, Germany, ...)
- **Last version (SAMPIC3) awaited for end of September.**

R&D µ-elec & systems



Patented in 2009



Our interest in Belle II

- **The department has a long experience in participating in large international projects**
  - Our technical developments cover all the fields involved in particle physics experiments
    - µ-electronics (analog & digital)
    - Board design
    - FPGA & Firmware (mostly ALTERA and ACTEL)
    - Control and acquisition software

- **SERDI already contribute to ARICH commissioning (L. Burmistrov)**

- **We are interested in joining the effort for the upgrade of BELLE II TDAQ**
  - Discussion about the different options for a new architecture of the COPPER boards
  - Hardware design
  - Firmware development: for us, this should be kept for well defined and non evolutive tasks requiring high speed and throughput, and leave the remaining part to software.

- **We could also participate in a potential FEE upgrade**