SVD Status

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August 24, 2017

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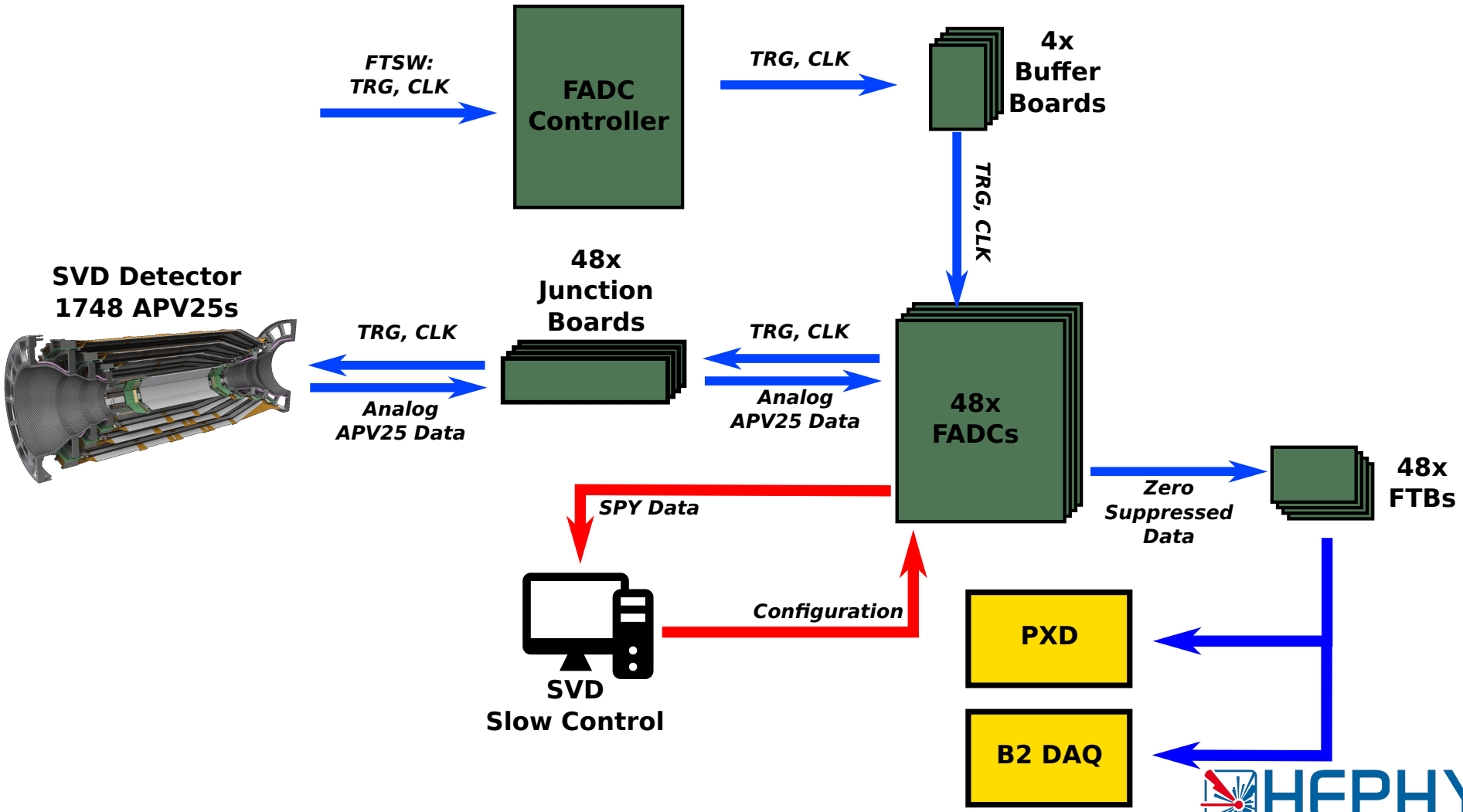
Overview

SVD System



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Outline

1. Ladder mount
2. Ladder production
3. Commissioning
4. Electronics
5. Software

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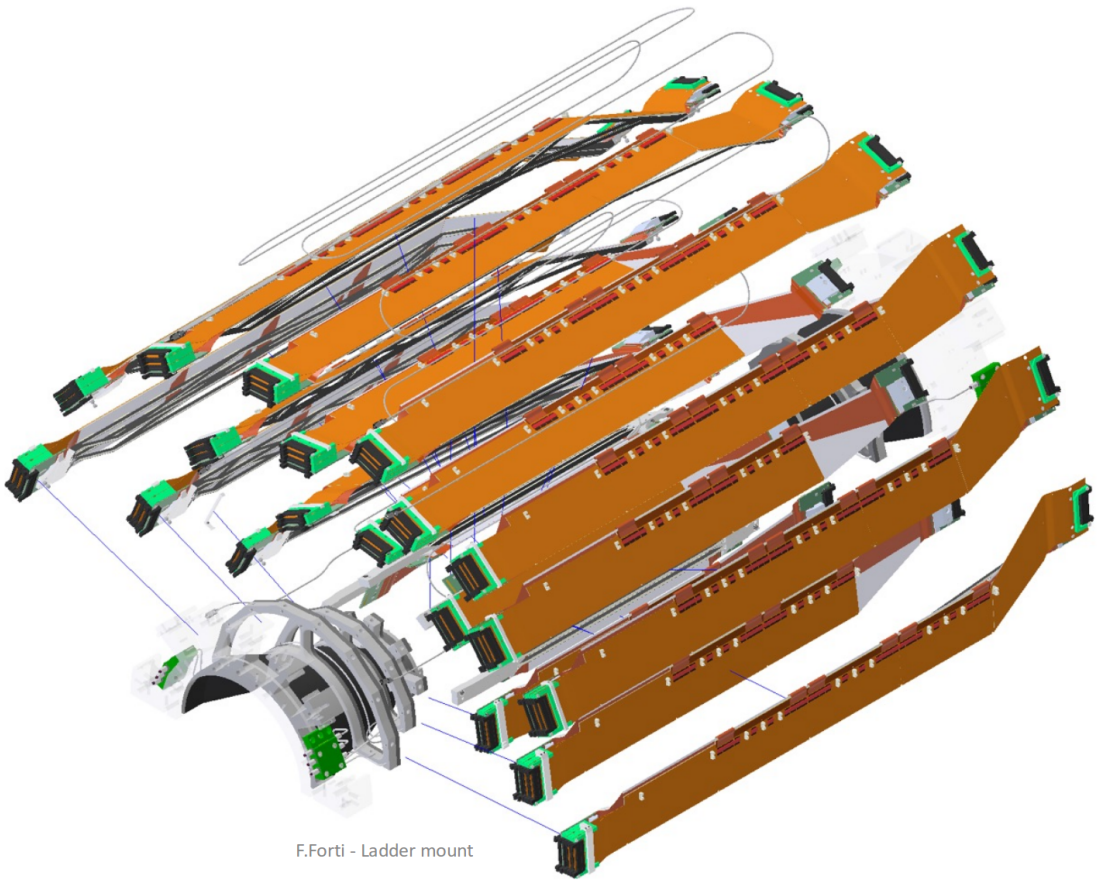
Ladder Mount

Preperations for the first half shell



- Optimizing the procedure for each layer and recorded the steps in a checklist.
- Four FADCs and junction boards to check the ladders after mounting.
- Software has been prepared.
- Each step in the procedure is extensively exercised by several operators and tested with class B/C/D ladders.
- 6th of September 2017 there will be an additional review.
- The ladder mount starts at the 8th of September 2017.

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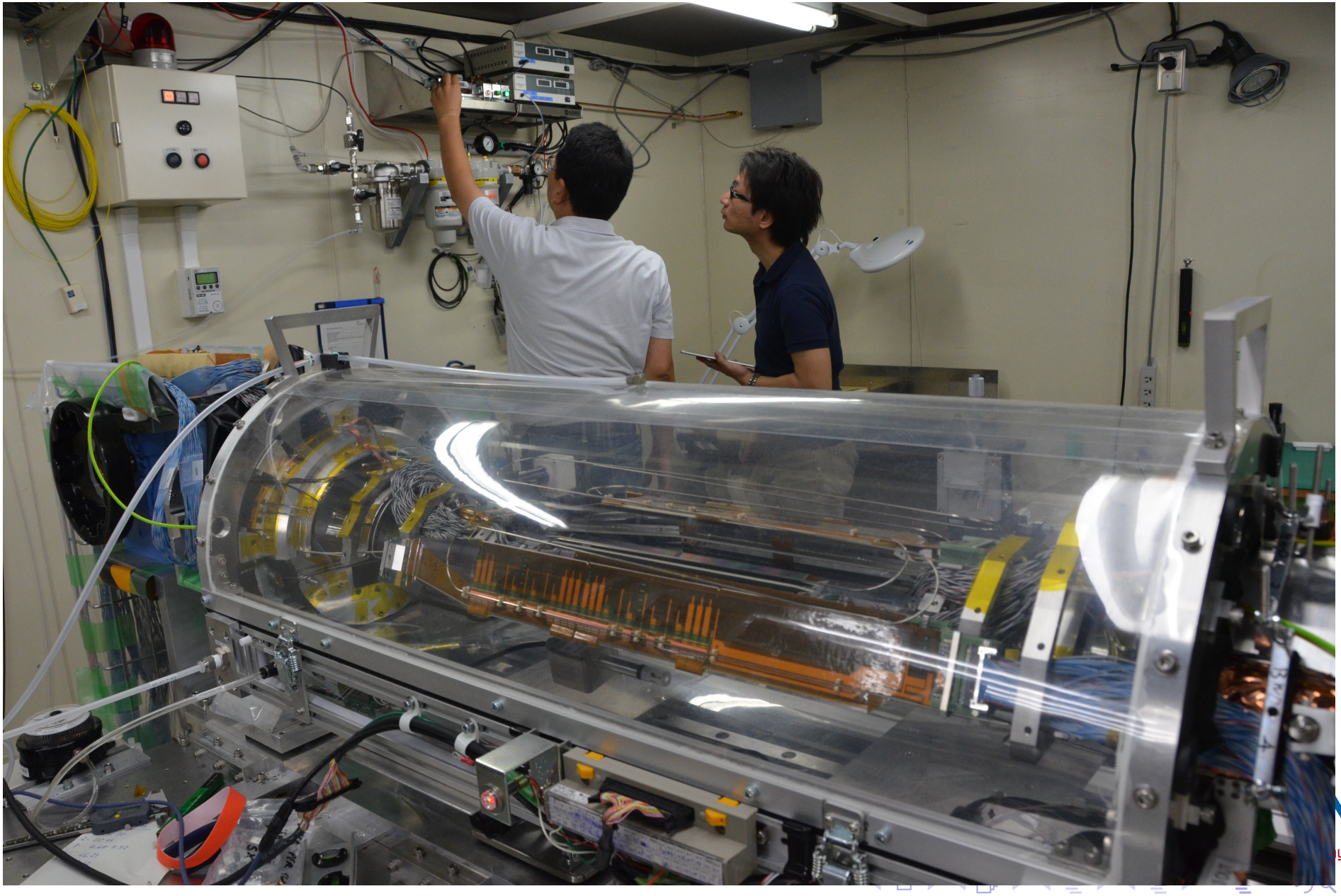
Ladder Mount

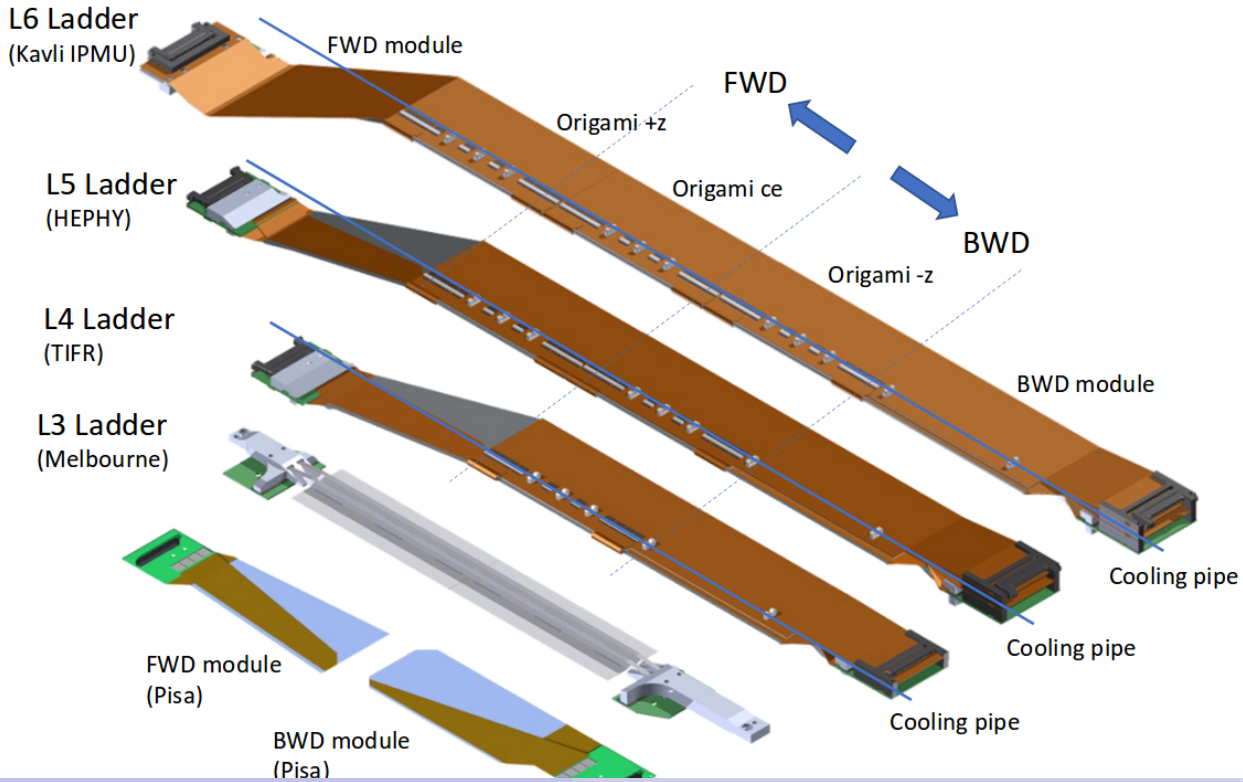


Ladder production

Status

Production status:

Production Sites	Class A	Required(+spares)	Half Shell Mount	Completion
PISA (FW, BW)	47, 47	—	—	**done**
Melbourne (L3)	11	7(+2)	ready	**done**
TIFR (L4)	6	10(+2)	ready	10.2017
HEPHY (L5)	13	12(+3)	ready	09.2017
Kavli IPMU (L6)	8	16(+4)	ready	03.2018



Commissioning

Phase 2 milestones:

- **19 Sep - 25 Sep:** PXD/SVD DAQ integration test w/o detector
- **22 Sep - 17 Oct:** Phase-2 VXD detector integration
- **11 Oct - 17 Oct:** SVD installation and test
- **19 Oct - 01 Nov:** Phase-2 VXD commissioning
- **7 Nov:** Phase-2 VXD installation
- **28 Nov - 11 Dec:** Installed phase-2 VXD commissioning

Phase 2 TODOs:

- Operation at 30kHz

Phase 3 TODOs:

- FADC V3 vs V4 comparison and mass production.
- FADC Gb Ethernet readout
- Remote FPGA flashing.

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Electronics

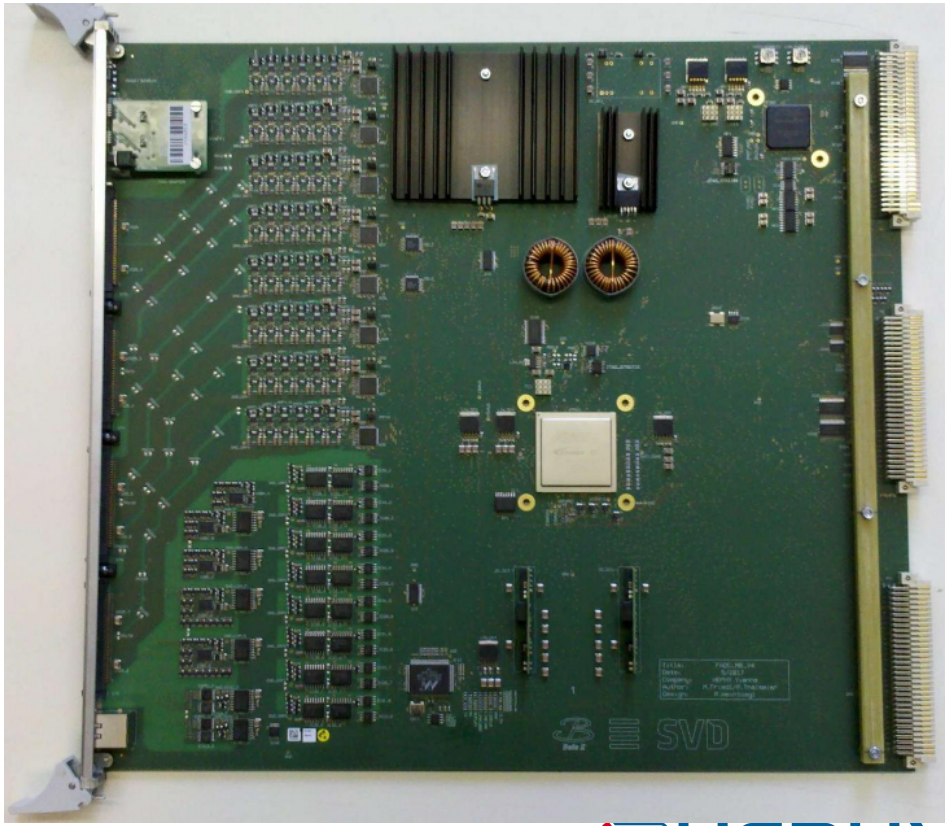
FADC V4

The main motivation for the V4 update was to make the FADC system more noise resistant than V3. We applied the following upgrades:

- Merging p/n-side FADCs, to eliminate the ground loop caused by a split readout.
- Additional noise filter in the APV25 power lines on the junction board.
- HW watchdog to release VME access, needed for remote flashing.
- Better protection of the FADC inputs, ie against HV shorts or electro-statical discharges.
- Better electrically protected monitoring readout
- Issues found in the V3 has been corrected, ie Gb Ethernet, JTAG daughterboard, ...

Status:

- V3 and V4 comparisons will start at the 17th of September.
- Remote flashing is implemented in the firmware, the software counterpart has to be developed.
- The Gb Ethernet has been tested but a specialized firmware code and software updates are not done yet.
- No major HW on V4 issue found. (Few LEDs on the GbE module was soldered the wrong way...)



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Electronics

Trigger Veto

One of the major phase two item is the trigger veto module. Every other HW module is ready for the 30kHz readout.

Hikaru Tanigawa is working on implementing the SVD trigger veto module in FTSW. The module monitors incoming triggers to evaluate the occupancy of APV25 buffer. The estimated dead time simulated with a C code yields:

- 30kHz - 6 frames: 2-3%
- 40kHz - 6 frames: 12%
- **30kHz - 3 frames: $>$1%**

Development Status:

- Using a Mersenne twister to generate the Poisson triggers, confirmed the dead time yielded by the simulation.
- The next step is to test the trigger veto implementation with a Origami module.
- Expected to be ready before the DAQ test at 19th of September.

Note: Just tested FADC V4 with a origami module with 3 frame at 32kHz pulsed trigger without trigger veto.

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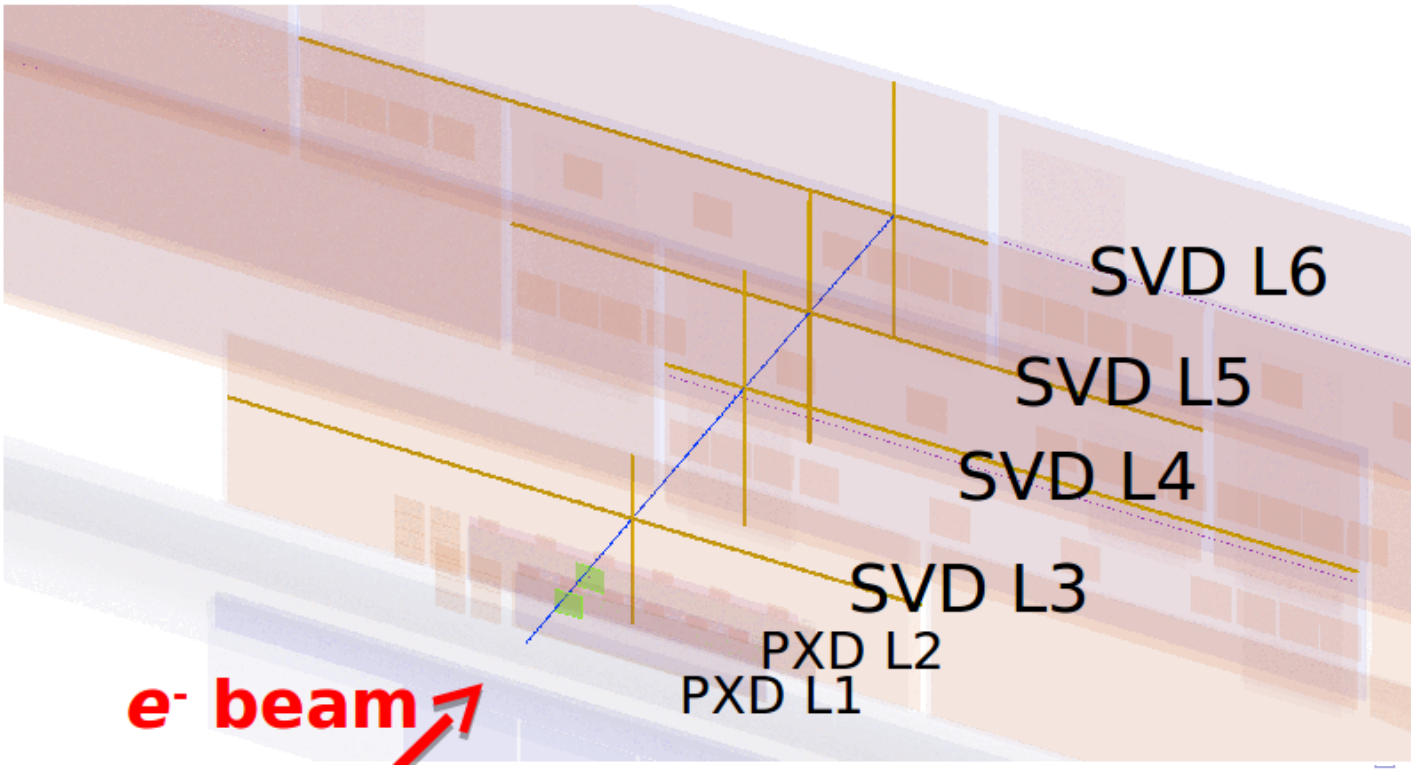
Software

Offline Software

The offline software group is currently aiming to refactor and extending the exiting reconstructions codes:

- `SVDNNShapeFitter`: Neural network fitting the hittime and amplitude of the particle signal.
- `SVDClusterQualityEstimator`: Quality of the cluster data.
- Interface to read from the condition database.

Expected release of `release-01-00-00-branch`: November 2017



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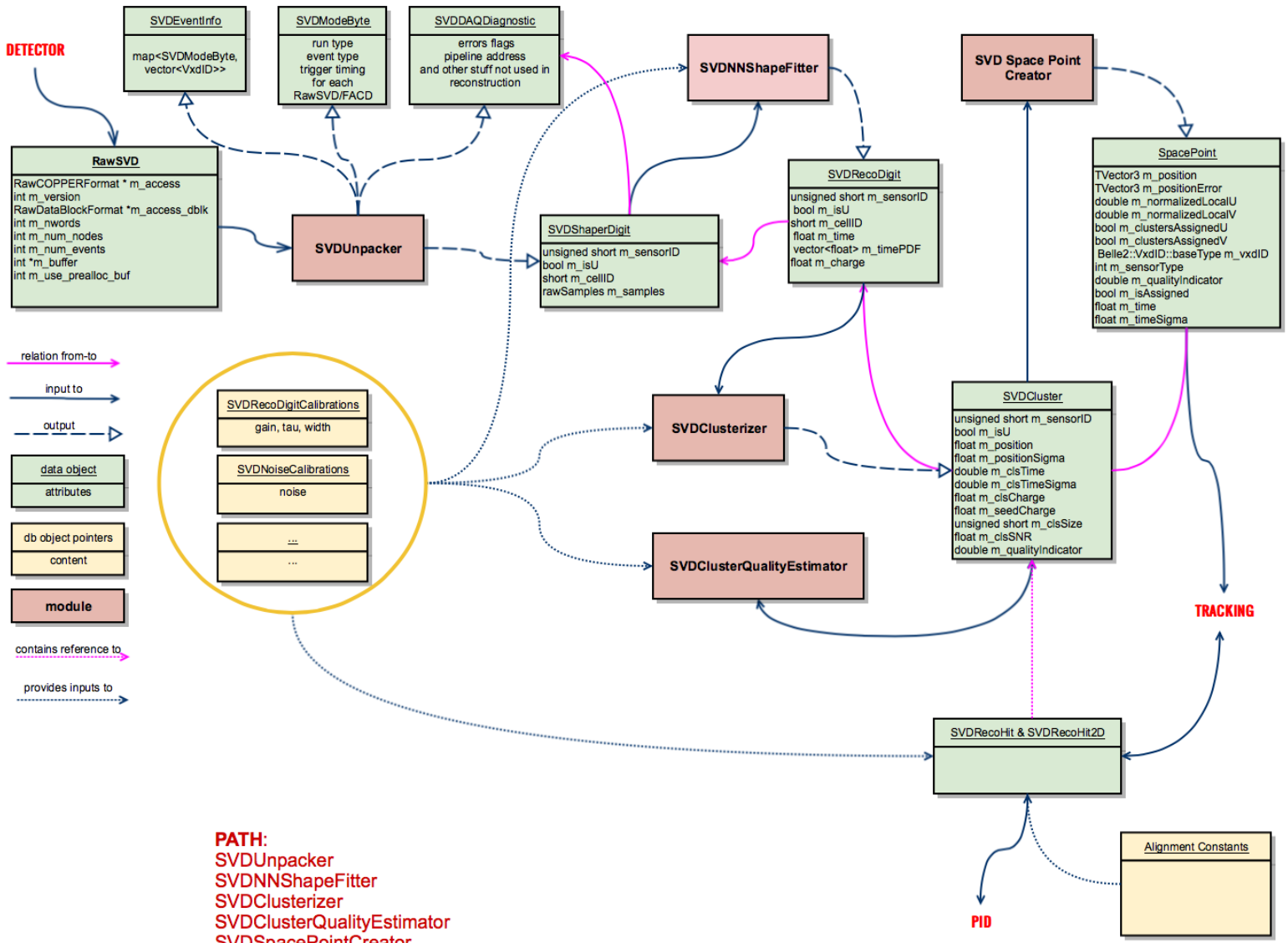
Software

Offline Software



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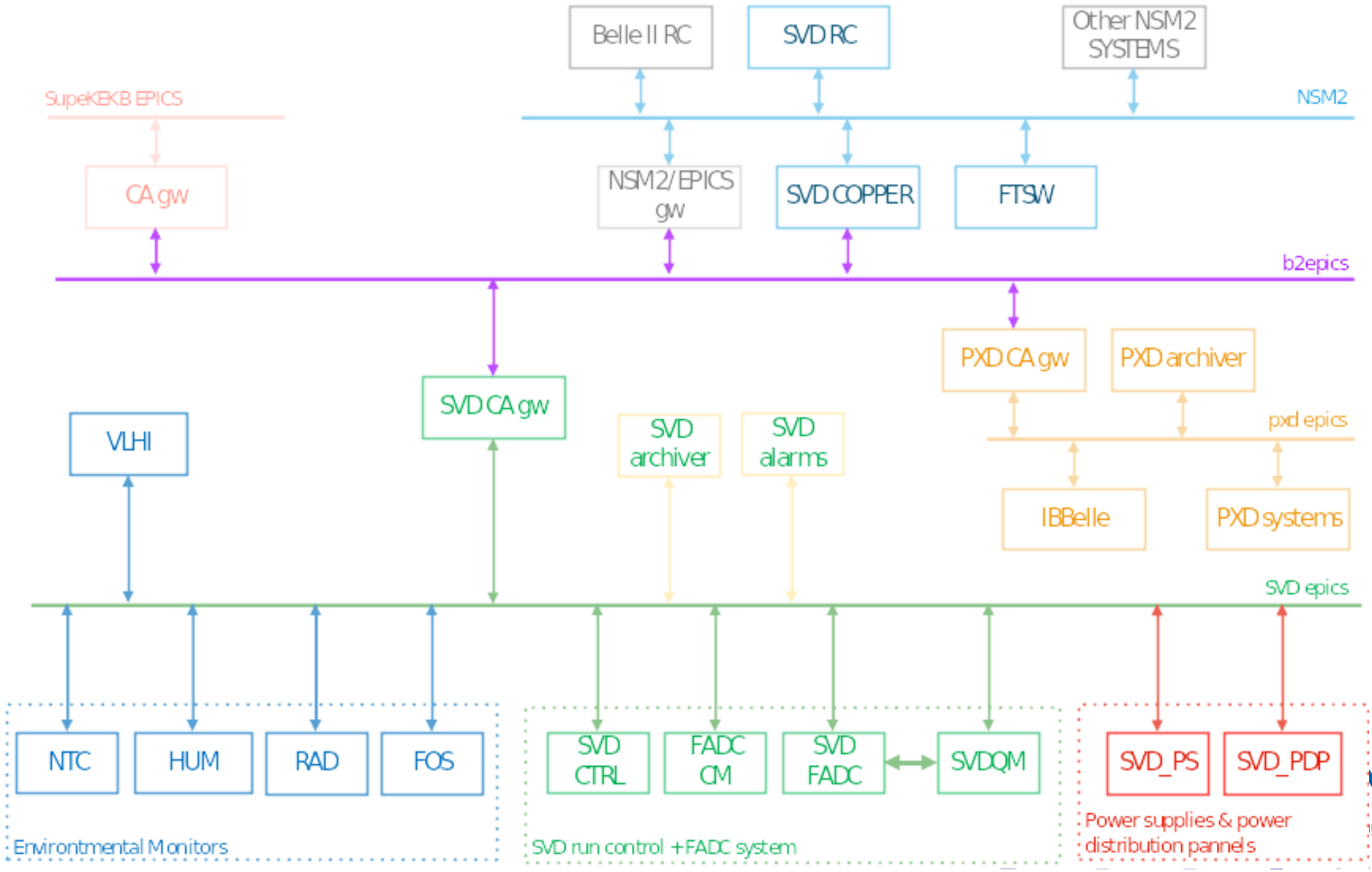
Software

Online Software - Slow Control



Status:

- We added a revised `SVD:PS` module with different operation types and configurations to support V_{SEP} and IV scan of each connected sensor.
- The `SVD:FADC` and `SVD:QM` have been updated to readout and evaluate those run types.
- The slow control has been updated to work with FADC V3 and V4. In order to distinguish between those two versions the following has been defined:
  - V3 FADC ID: `0b00XX'XXXX` = p-side and `0b10XX'XXXX` = n-side
  - V4 FADC ID: `0b01XX'XXXX`;
    p-side: `mod(APV25 ID, 6) == even`
    n-side: `mod(APV25 ID, 6) == odd`
- For phase II we will use the XML file based configuration, but we currently working on a standalone software to convert and upload the XML files to the condition database.

PS PDP will arrive at KEK in September, the `SVD:PS` extension will developed on site.

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Software

Slow Control - Main OPI

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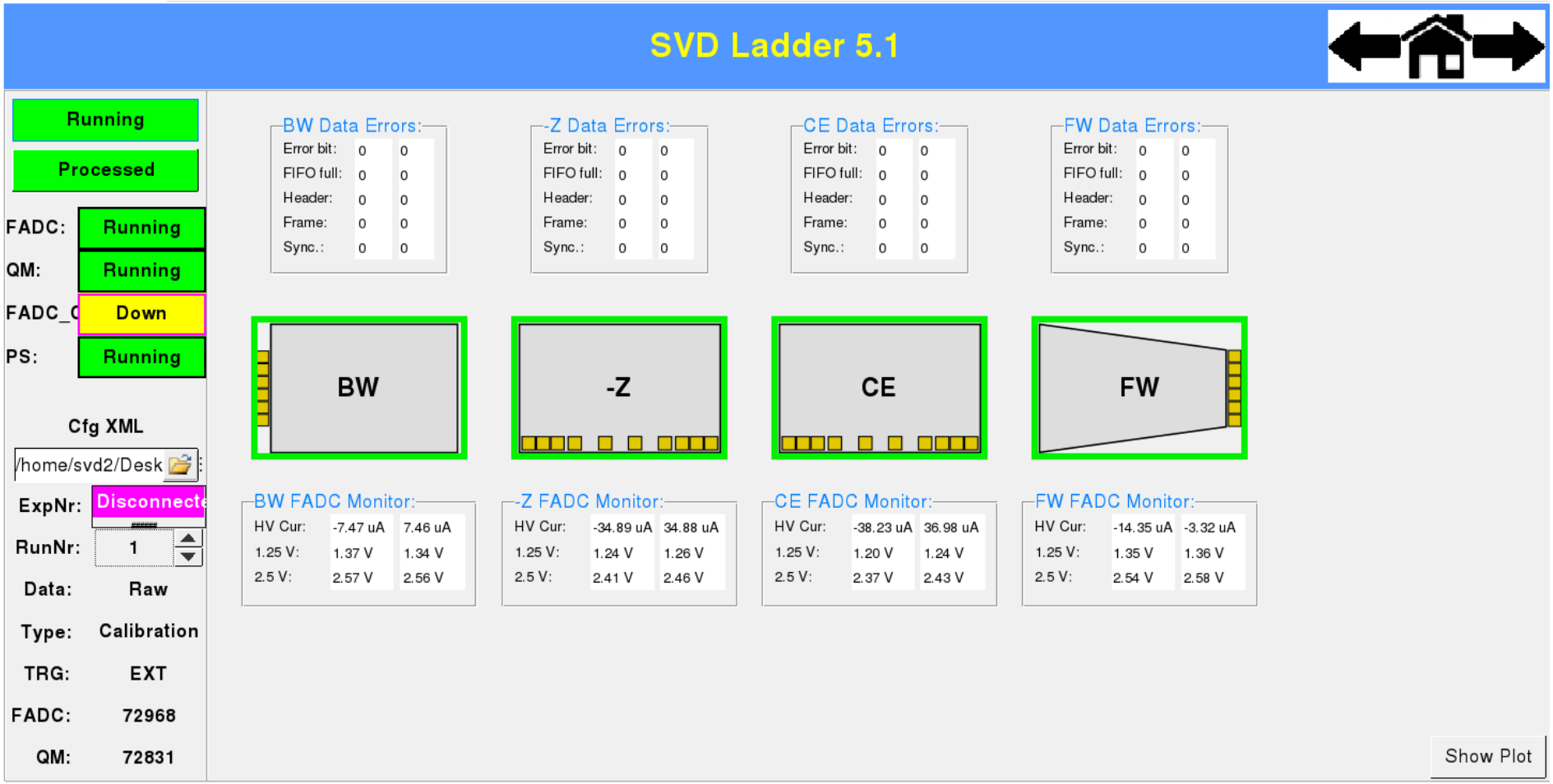
Software

Slow Control - Ladder OPI



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Summery

- We are improving the Ladder mount procedure to minimize the risk.
- FADC V4 prototypes are tested and no major "show-stoppers" found yet.
- The trigger veto module is currently developed, the current state shows promising results.
- Offline software is aiming to refactor and upgrade the tracking code.
- Online software is working on the condition database and PS PDP upgrades.

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Thank you!

Questions?

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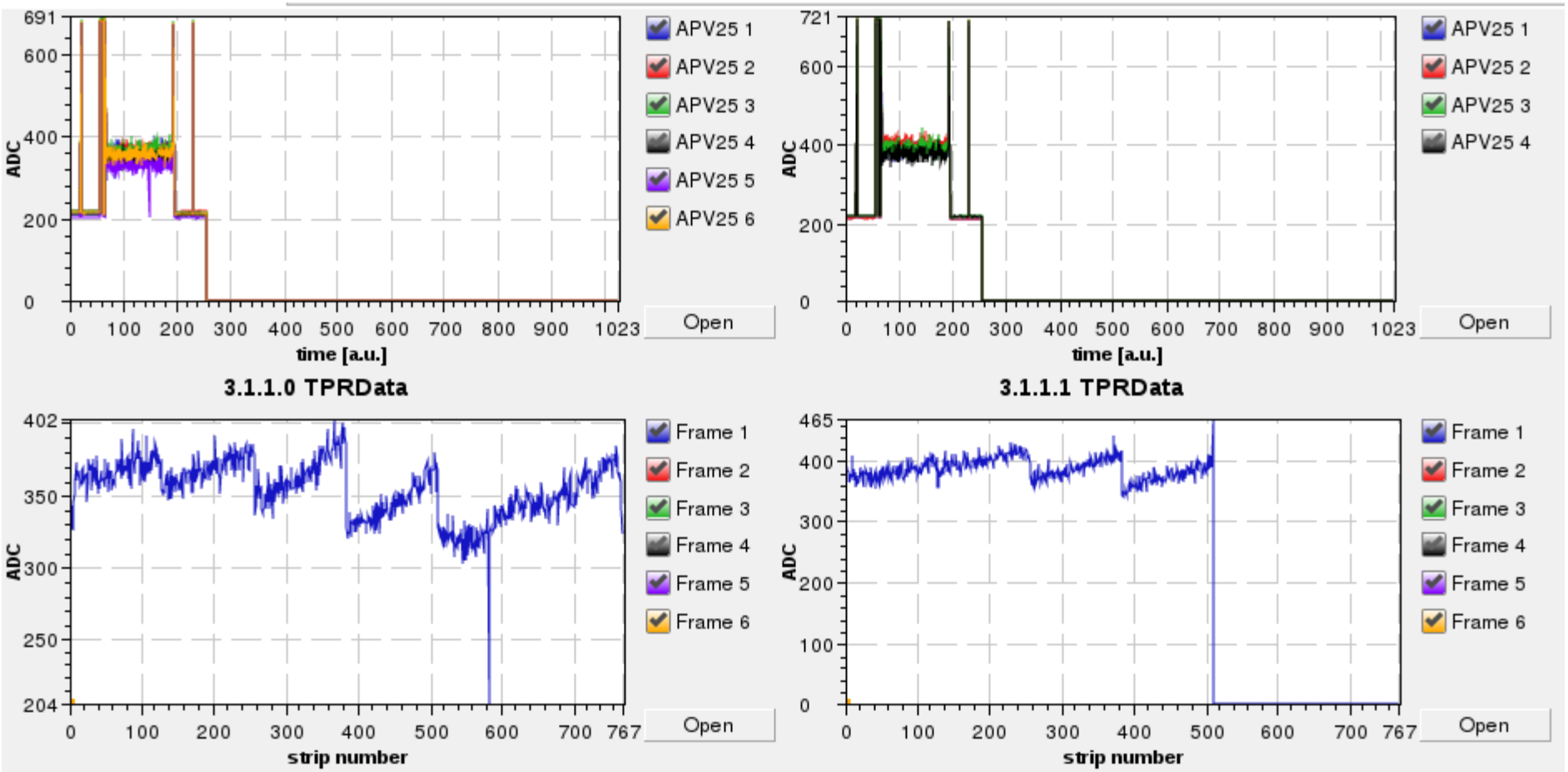
Backup

Slow Control GUIs



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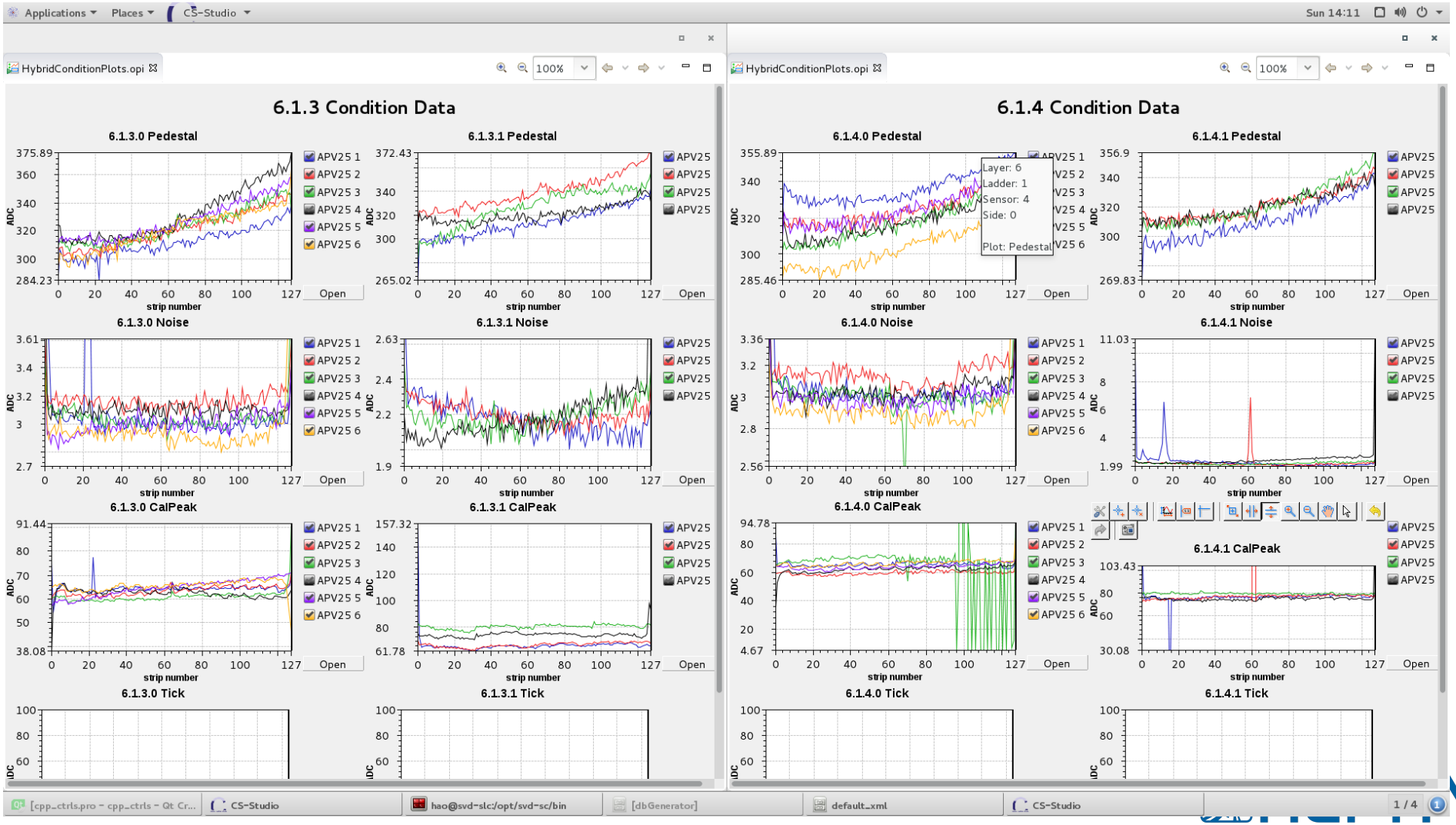
Backup

Slow Control GUIs



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