Status on ETM

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TRG DAQ Workshop

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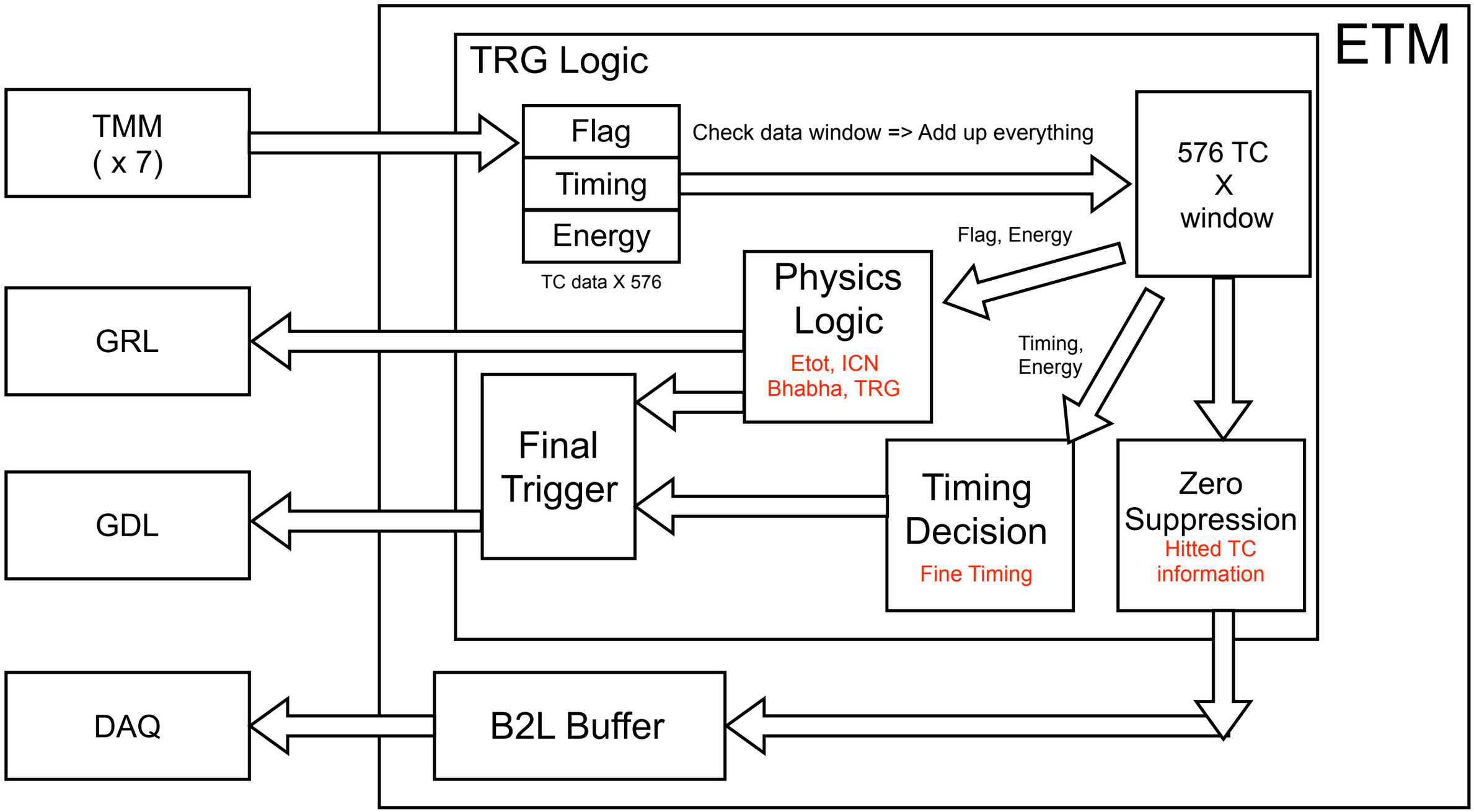
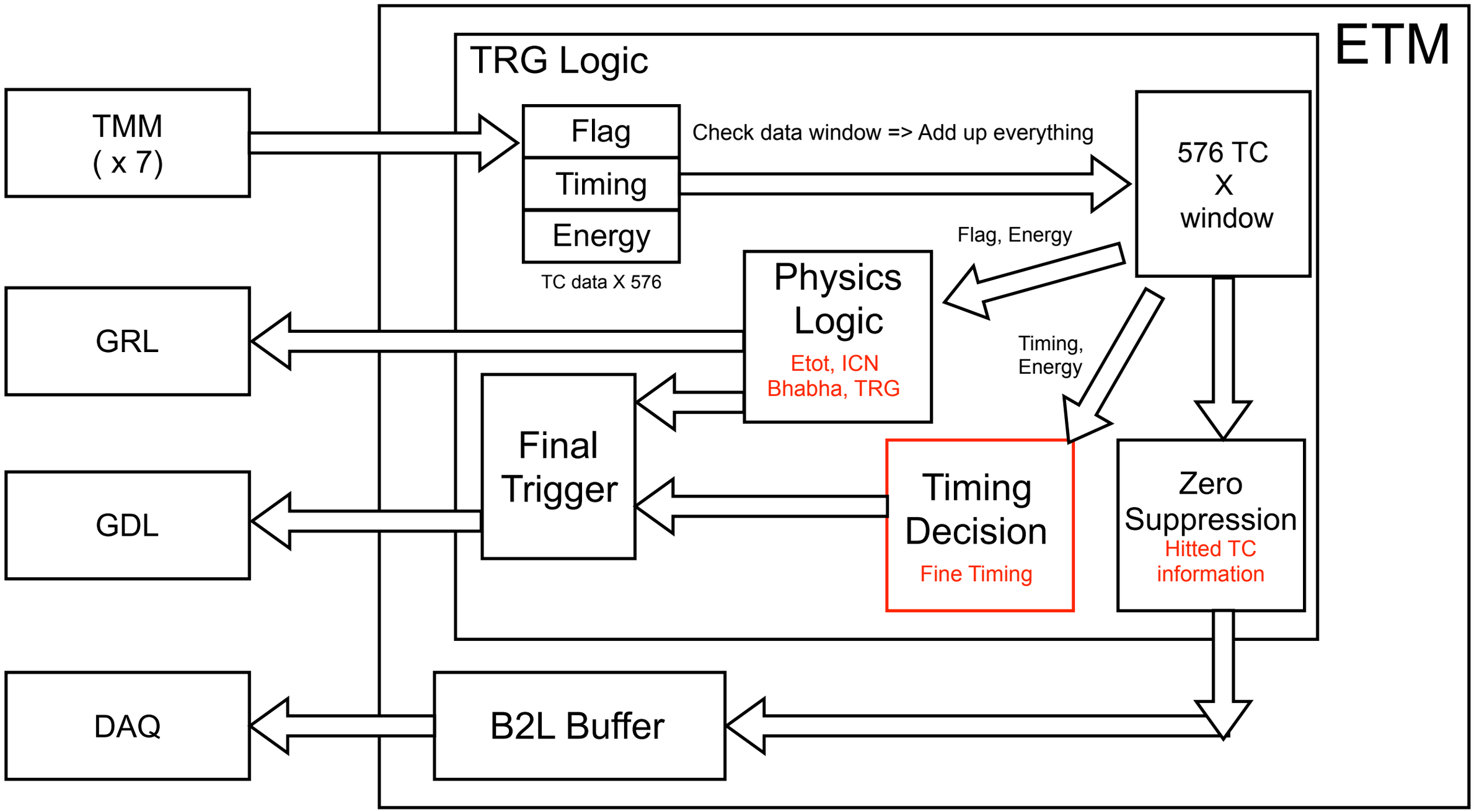
ETM Trigger Flow Chart



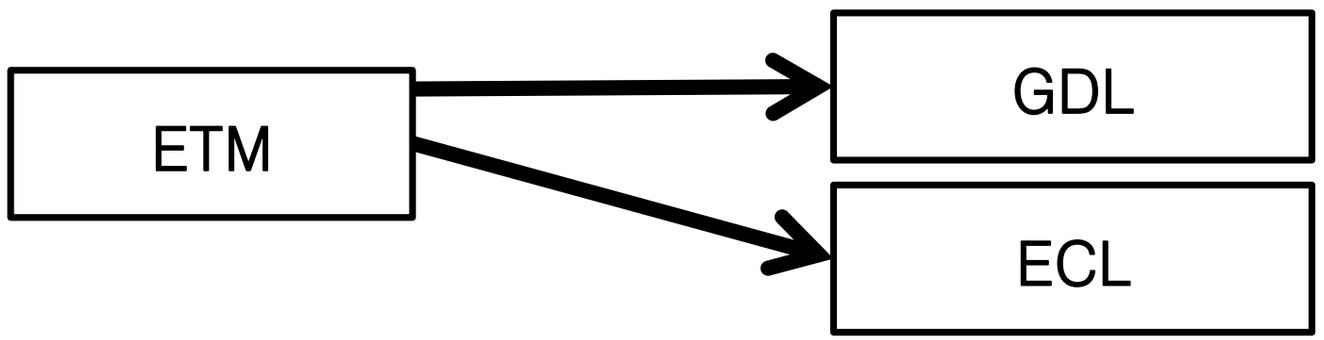
ETM Trigger Flow Chart

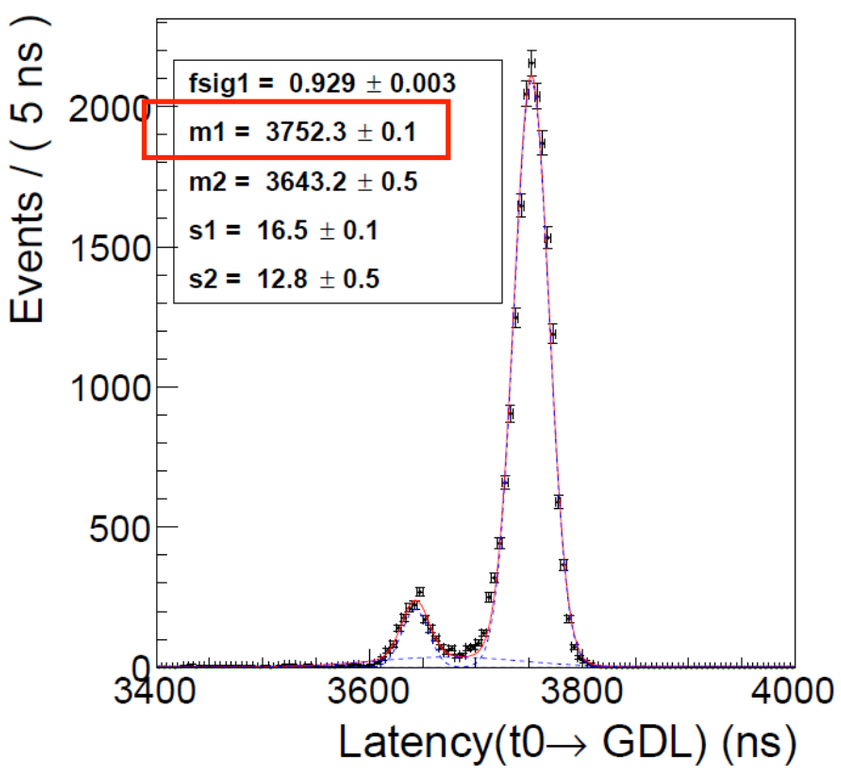


Latency Check

- Measure latency from Scintillator to GDL @ Detector by Nakazawa-san.

Double peak ecltrg trigger timing



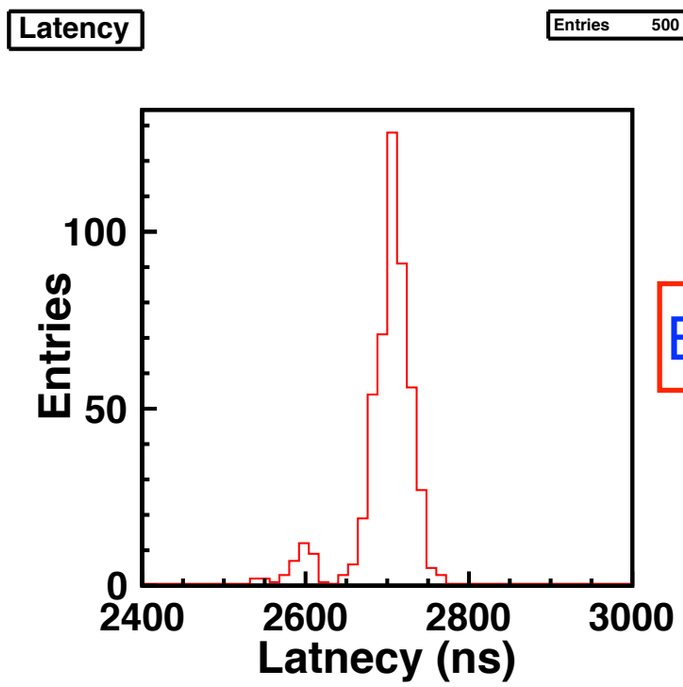


- Double peak trigger timing was found by GDL and reported by Nakazawa-san.
  ~125ns timing difference.
- Alex also reported ~100ns trigger timing in ECL data taken based on a trigger by only ECL trigger.
- Confirmed double peak trigger timing at B2 setup.
- Found in CDC data by Taniguchi-san too.
  - But actually triple peak in CDC data…

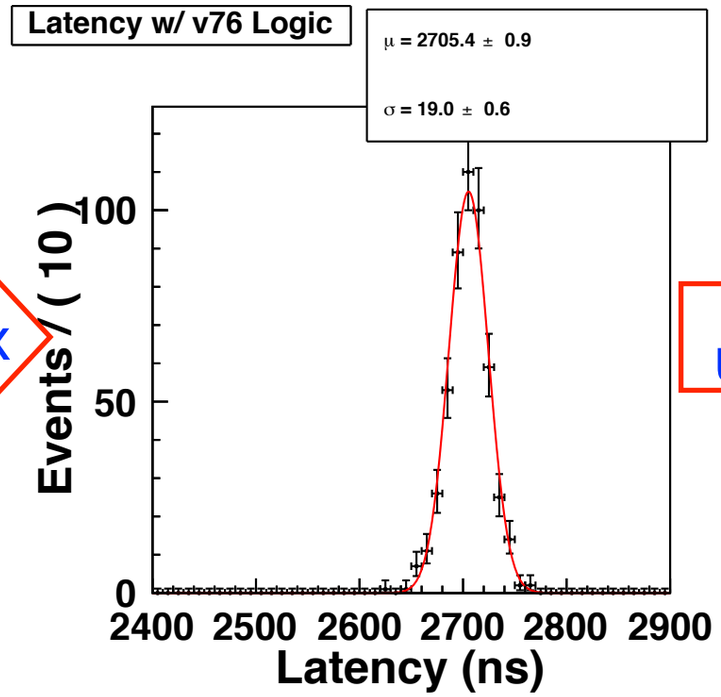
ECL-Meeting : 12th May, 2017

Update Logic and Measure Latency

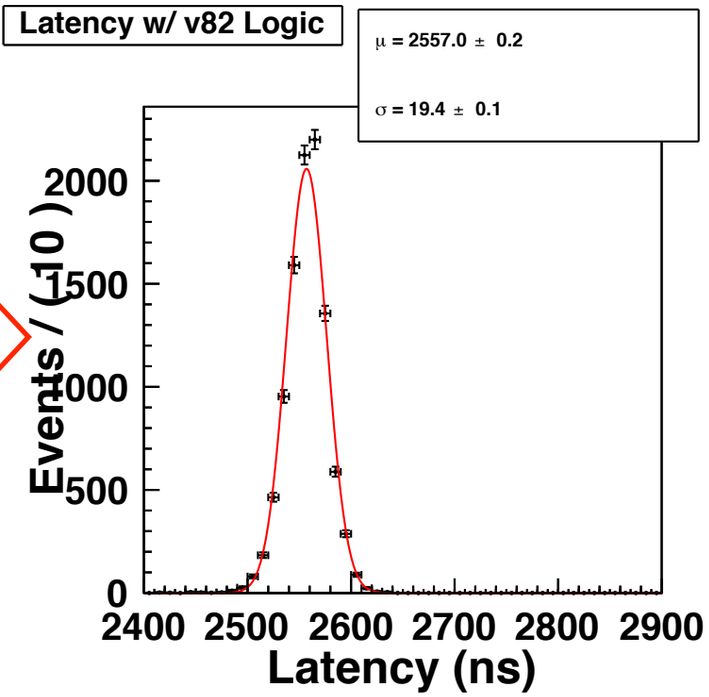
1. Fix the double peak problem
2. Update TRG Logic
   - Using B2 setup, we got improved latency.



Bug Fix



Logic Update



Latency (ns)	EH	B2
Old	3752.3	2705.4
New	????	2557.0

148.4 ns

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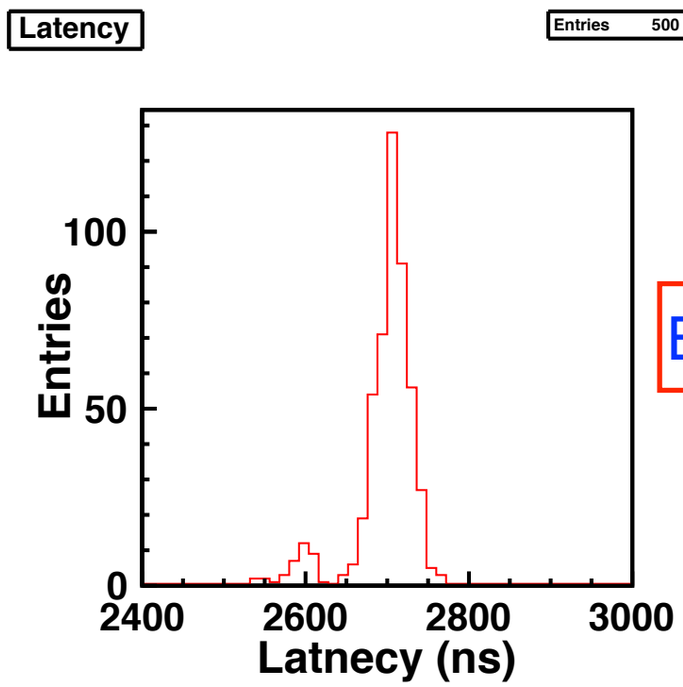
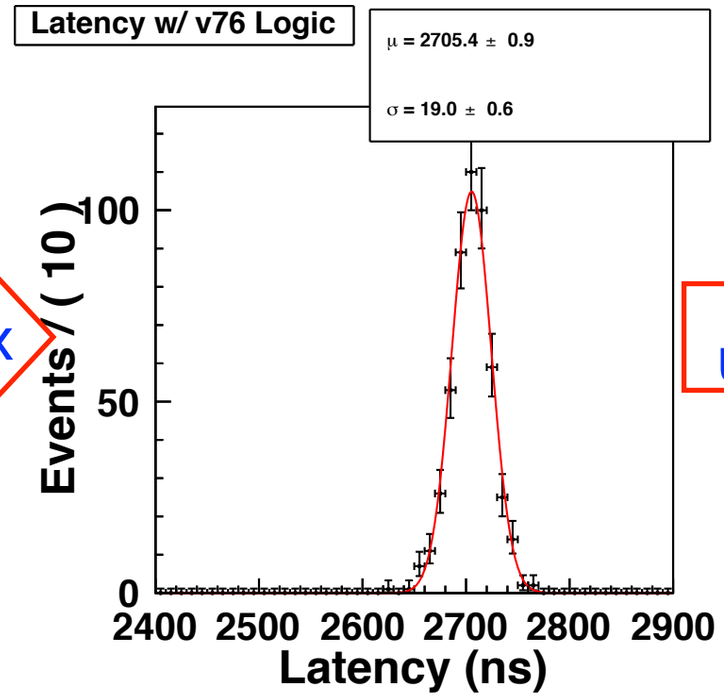
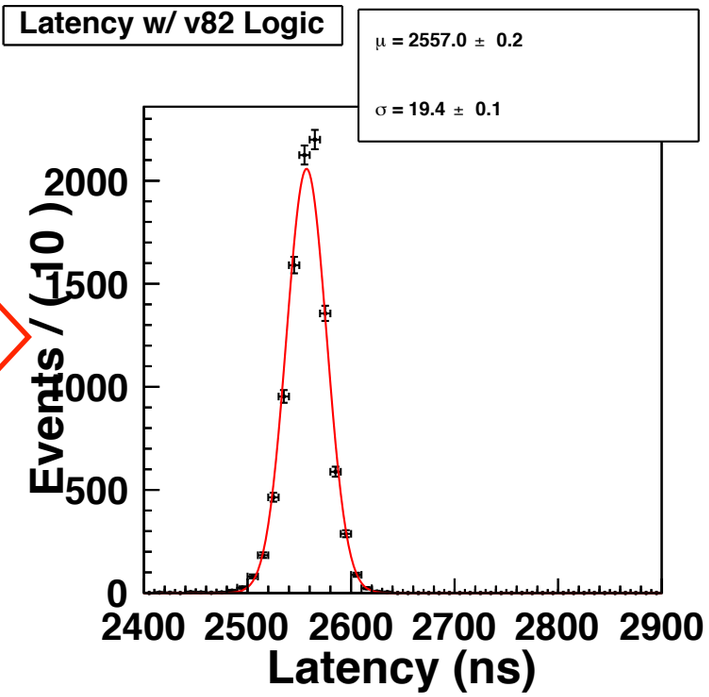


Bug Fix



Logic Update



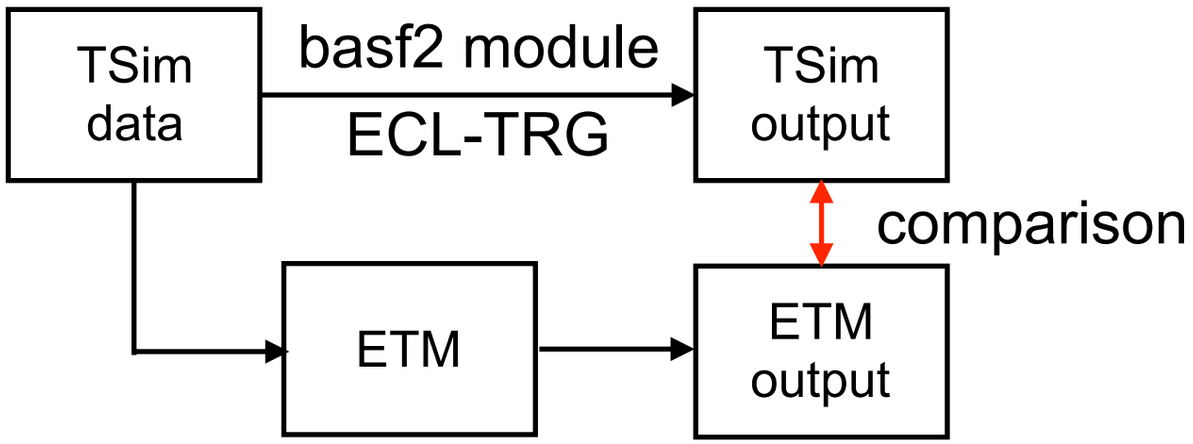
Latency (ns)	EH	B2
Old	3752.3	2705.4
New	3603.9 (expected)	2557.0

148.4 ns

Expected Target Latency :
3800 ns = 3600 + α (bhabha + physics + etc)

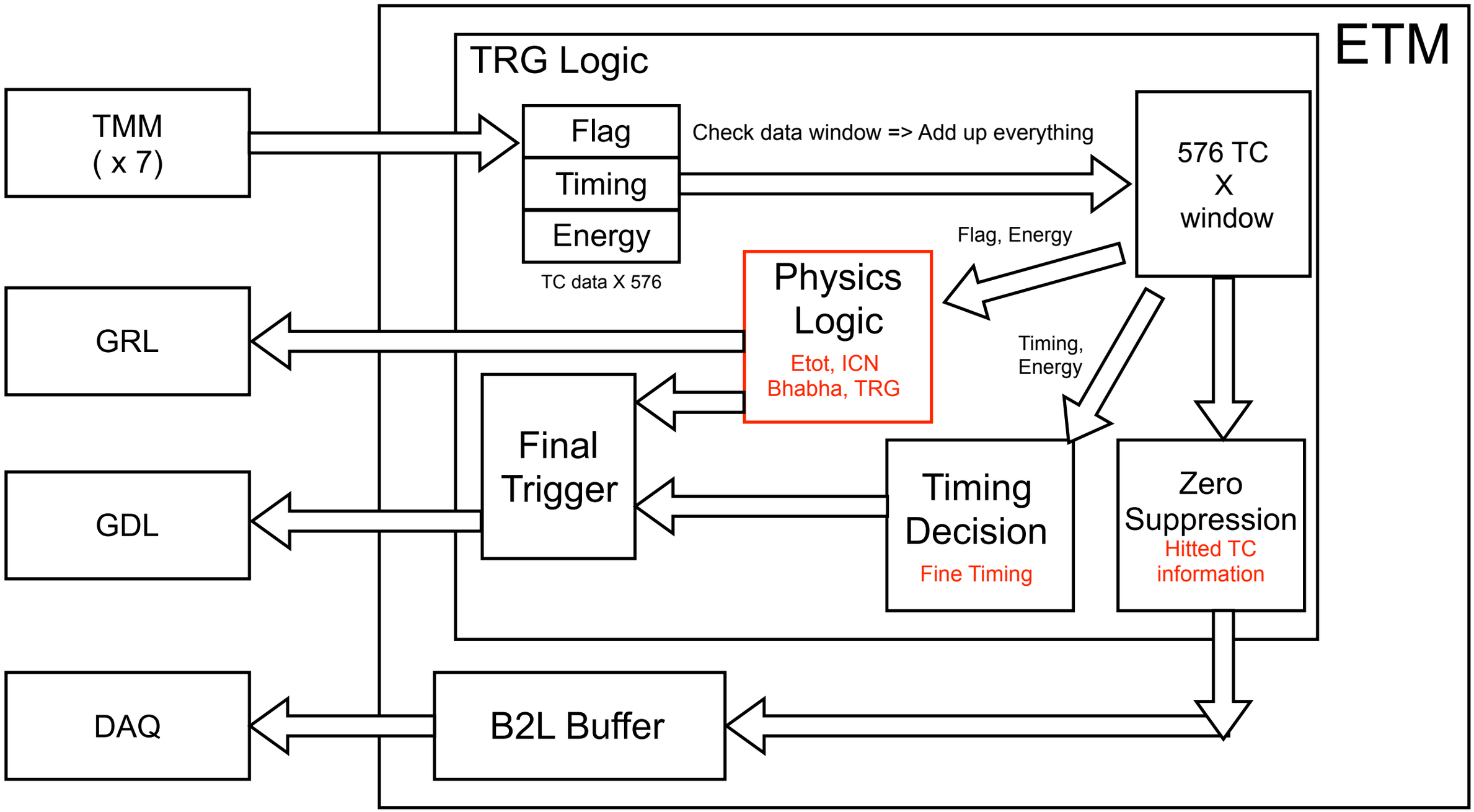
TSim Study

- In order to check the performance of new ETM logic, we prepare TSim study.
- Add BRAM to ETM firmware for storing TSim data.
- I.S. Lee prepare TSim data
  - Condition : 10K Bhabha events, 10K Y(4S) events w/o Beam BG
- Compare the output of ETM firmware and TSim result.



- We have got 99.9% consistency btw TSim & Firmware.
  - All inconsistent events occurred because of different data type btw Real(TSim) and Integer(Firmware)
    - Integer type TSim or Firmware simulator is needed.
  - Here, we compare three items
    - Bhabha TRG signal(on/off), ICN, and Total Energy(GeV, second decimal place).

ETM Trigger Flow Chart



Belle I type Bhabha Logic

- Belle I type Bhabha logic is prepared in ETM firmware.

ϕ-ring combinations in Belle II enviroment

Barrel

C12	C11	C10	C9	C8	C7	C6	C5	C4	C3	C2	C1

B1
B2

Backward

Combination (θ id)		Energy cut (F, B : GeV)	
F1 + F2 + F3	B1 + B2	3.5	1.0
F3	C12	3.0	1.0
F2 + F3	backward gap	5.0	
C1	backward gap	4.0	
C1	C11 + C12	3.5	1.5
C2	C11 + C12	3.5	1.5
C1 + C2	C11	3.5	1.5
C2	C10 + C11	3.5	1.5
C2	C9 + C10	3.5	1.5
C2 + C3	C10	3.5	1.5
C2 + C3	C9	3.5	1.5
C3 + C4	C9	3.5	1.5
C3 + C4	C8	3.5	1.5
C4 + C5	C8	3.5	1.5
C5	C7 + C8	3.5	3.0
C5 + C6	C6 + C7	3.5	3.0
forward gap	C11 + C12		3.0
forward gap	B1		3.0

F3
F2
F1

Forward

by I.S. Lee

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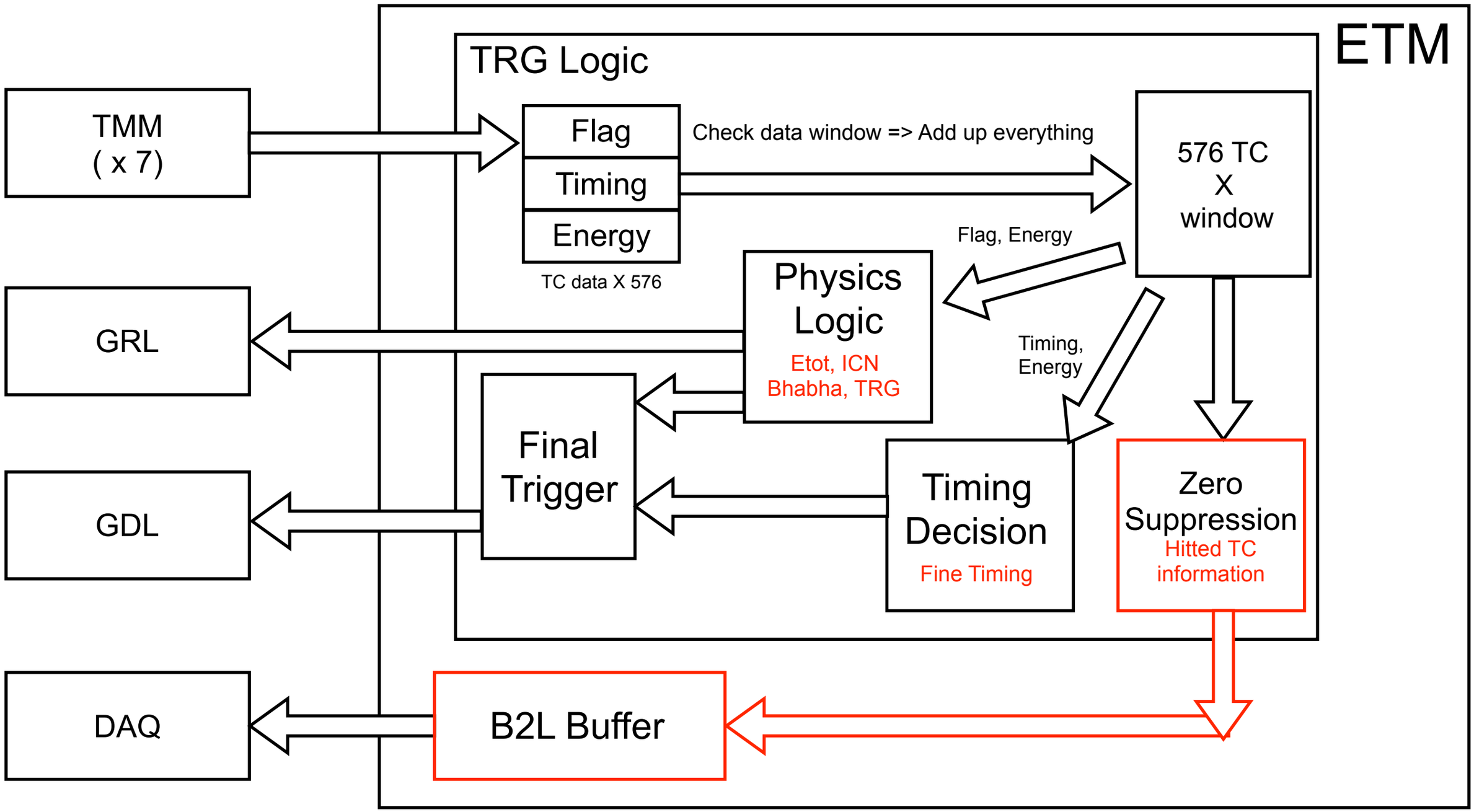
- Belle I type Bhabha Logic
  - Φ-ring sum with asymmetric energy cut
  - + ICN Logic (Belle I)
- Plan
  - Φ-ring sum(2D) ⇒ 3D
  - ICN ⇒ Cluster

ETM Trigger Flow Chart



Zero Suppression

- Current ECL-TRG data size to store daq copper is 12800 bit.
  - 576 TC × 22 bit (flag, timing, energy) = 12672 bit + α (R&D)
- Because of resource limitation in FPGA, ETM can't keep long data in B2L buffer.
  - Also timing constraint fit error was happened.
- We decide to reduce data size by suppressing unnecessary TC data.
- Max. # of TC Hit in Total (in firmware) : 63 (if needed, can increase)
  - TSim : ~30 for Y(4S) w/ BG

- Current Data. : 576 × 22 bit (flag, timing, energy) + α ⇒ 12800 bit
- Suppressed Data :
  - (Max) 63 × 30 bit + α ≃ 2000 bit = (1/6) × current data
  - (Bhabha) 3~5 × 30 bit + α = 100~200 bit
  - (Y(4S)) 10~30 × 30 bit + α = 300 ~ 1000 bit
  - (30 bit = 10 bit TC ID, 8 bit timing, 12 bit energy)

- Using Chipscope, we check our new logic works well.
- B2Link Buffer update is needed.

Summary / Plan

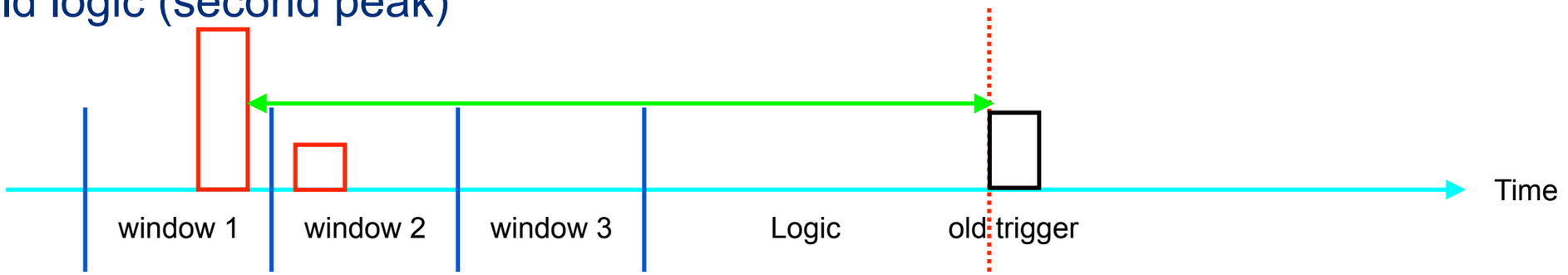
- ECL-TRG Logic Update
  - Double peak problem disappeared.
  - Reduce ETM latency.
- Belle I type Bhabha Logic.
- Zero suppression Logic is ready.
  - B2Link Buffer modification is needed.
- ETM → GDL : Fine timing (LSF = 1 ns) with ECL-TRG
- ETM → GRL : Dummy Data

- ECL-TRG Logic update
  - BG veto logic (~ 1 mon)
  - Clustering Logic (~ 1~2 mon)
    - 3D Bhabha veto logic (~ 1 mon)

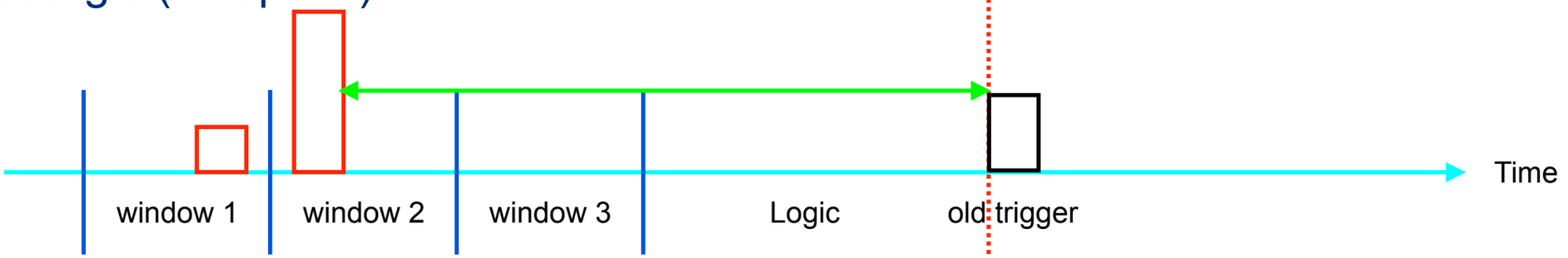
Backup

ECL-TRG Timing Decision Logic Update (1)

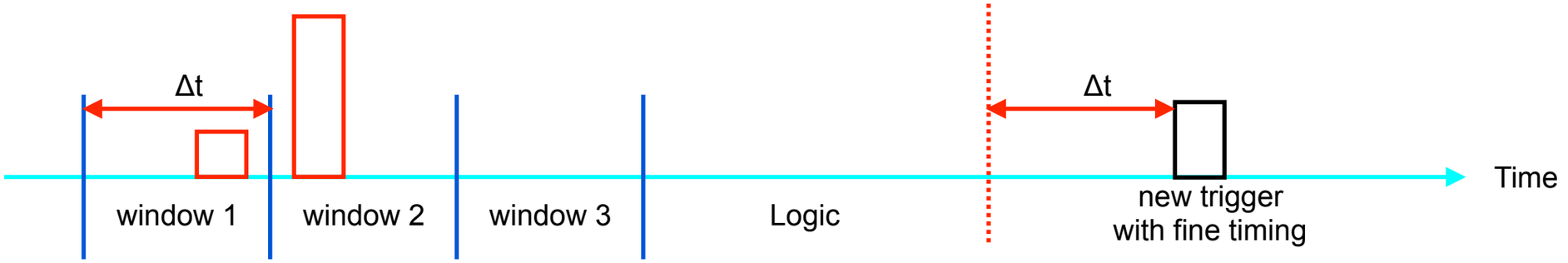
- Update trigger logic
  - old logic (second peak)



  - old logic (first peak)

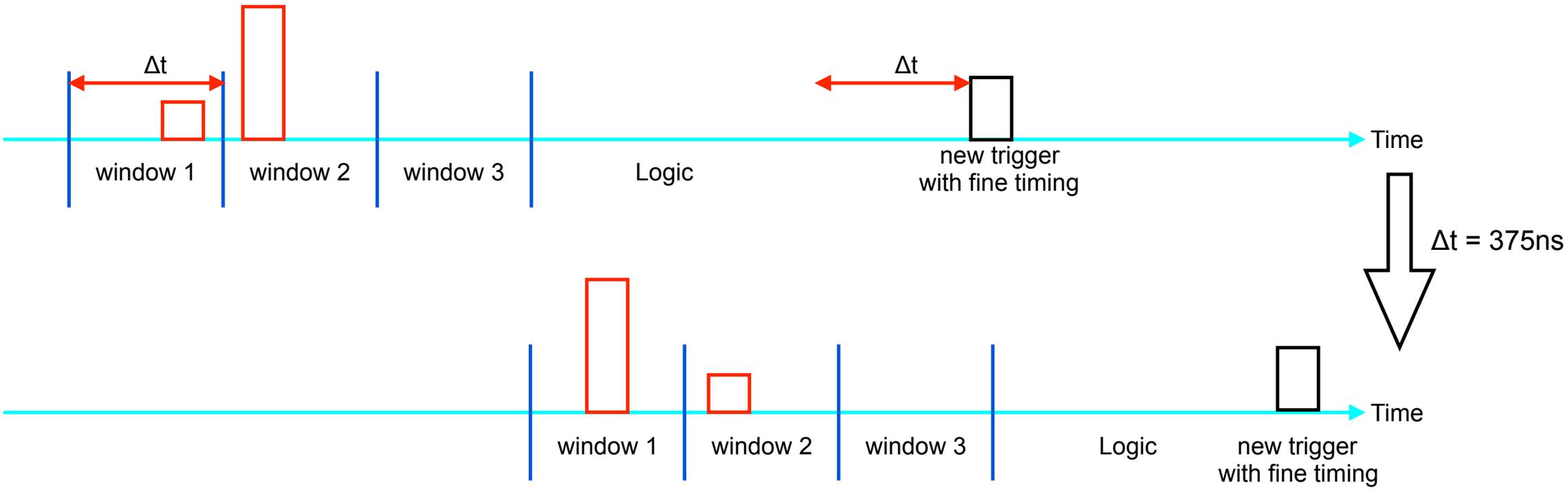


  - new logic (update)



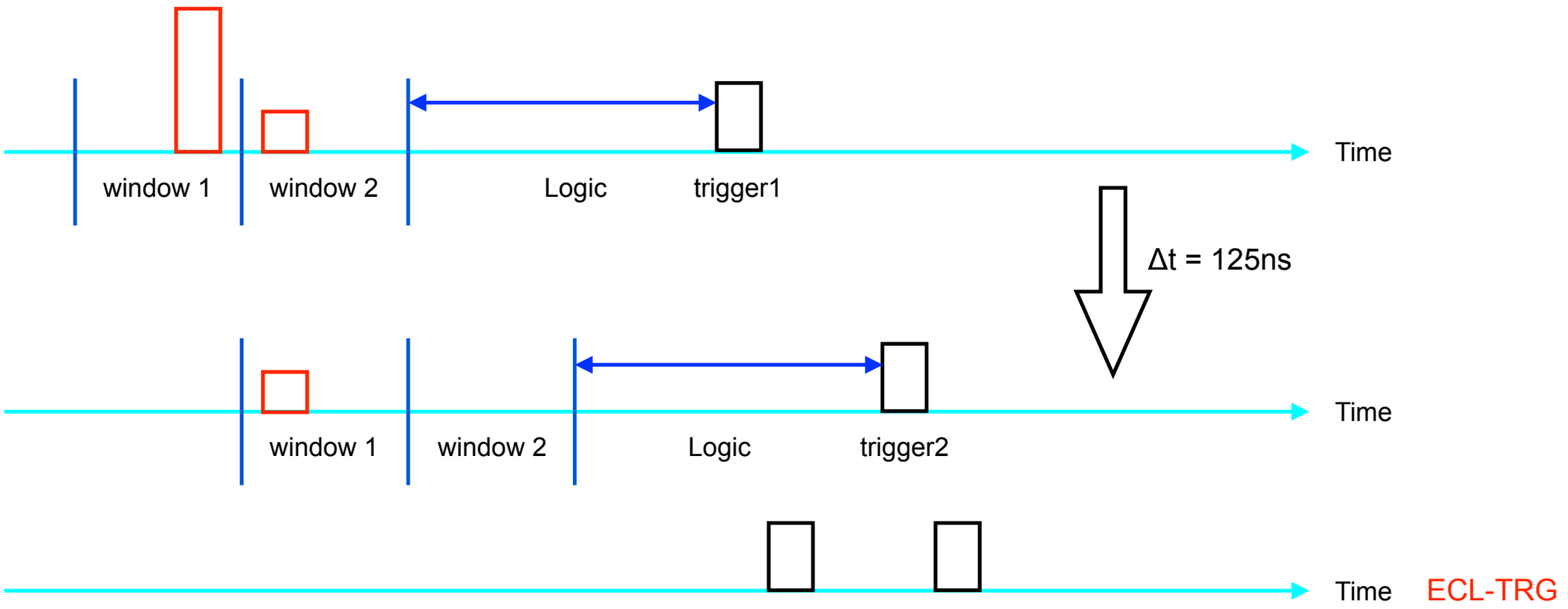
ECL-TRG Timing Decision Logic Update (2)

- I realize ETM timing decision logic is different from TSim logic.
  - Current Logic



ECL-TRG Timing Decision Logic Update (2)

- I realize ETM timing decision logic is different from TSim logic.
  - TSim Logic (case 1)



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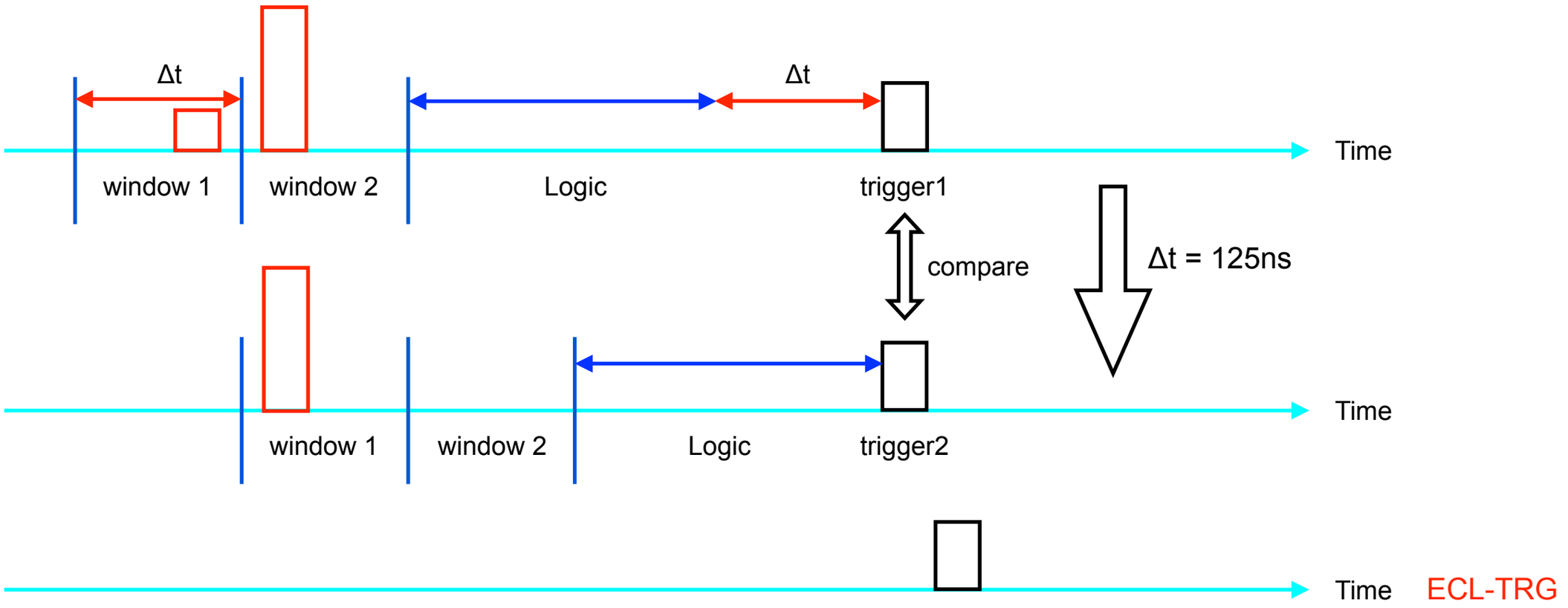
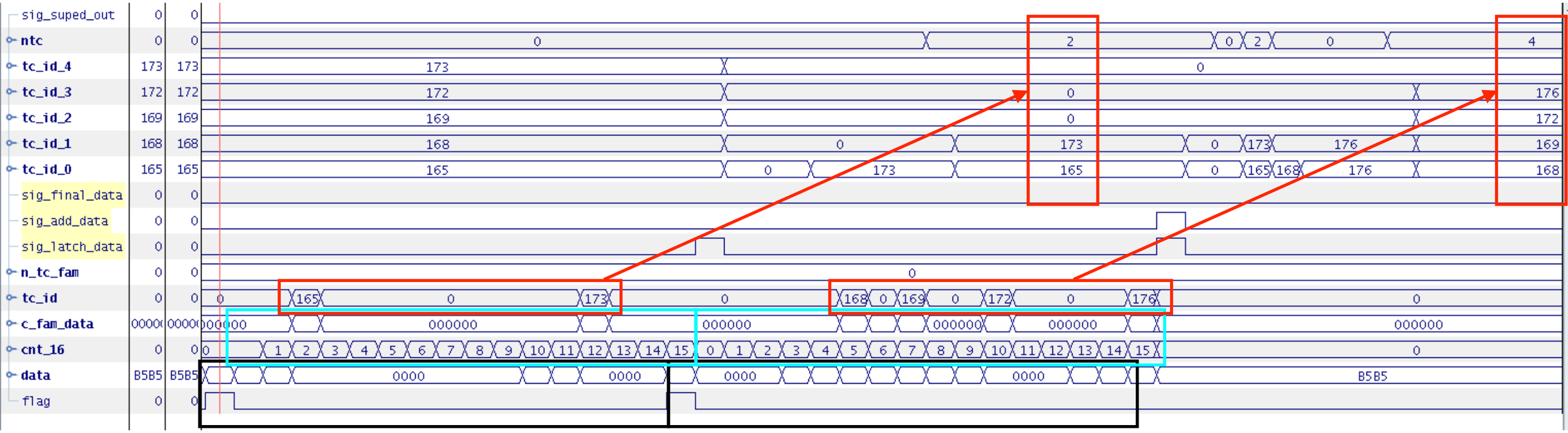
  - TSim Logic (case 2)



Result


sig_suped_out
ntc
tc_id_4
tc_id_3
tc_id_2
tc_id_1
tc_id_0
sig_final_data
sig_add_data
sig_latch_data
n_tc_fam
tc_id
c_fam_data
cnt_16
data
flag
2 hit
4 hit