

TOP Trigger Status

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- TOP counter is designed for barrel particle identification
- Its good intrinsic time resolution enables t0 (time of arrival of charged particles on TOP) estimation with ns time resolution
- $\bullet\,$ This t0 helps to reduce data volume of out-of-time hits in SVD

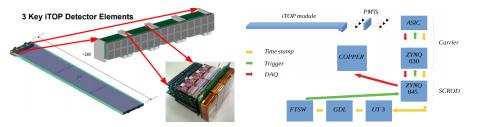


Image: A image: A

t0 estimation

- Timestamps: Time of arrival of photons on PMT
- Photons (timestamps) produced from a charged particle follow some pattern based on the location of hit on the bar

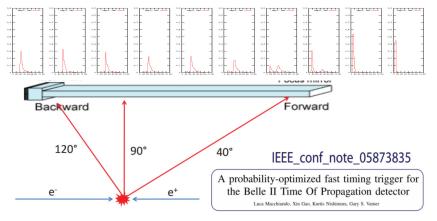
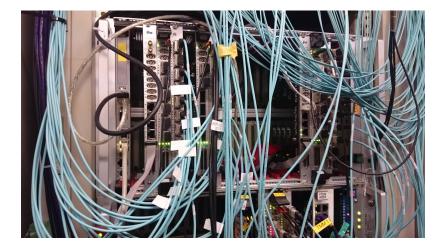


Image: A matrix and a matrix

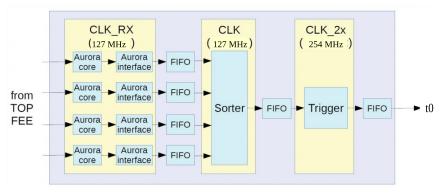


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- Timestamps are produced on FEE and send to UT3 using AURORA 8b10b protocol at a line rate 5.08Gbps.
- Timestamping is based on revo9 marker synchronized with the accelerator clock
- revo9 marker is updated every 90us
- Timestamp is represented by the number of clock cycles since most recent revo9 marker
- Clock used for timestamps allows 3ns binning. Therefore 16 bits are sufficient for timestamping (timestamping is done on both edges of axiClk(169 MHz). axiClk= 8 × SSTClk= 8 × FTSWClk/6, FTSWClk = 127 MHz)
- Timestamping at 1ns binning will improve trigger performance

TOP Trigger Firmware

t0s are estimated separately on each TOP bar and are combined later



- **9** Receive: Timestamps come through 4 channels from FEE
- Sorting: 4 channels are merged and Timestamps are sorted according to time
- O Trigger: t0 is estimated by fitting the Timestamps to PDFs by a Maximum Likelihood Fitting

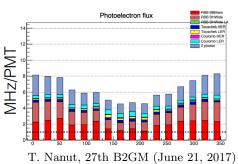
- TOP Trigger FW for single Bar is tested at KEK and estimate trigger rate
- $\bullet\,$ FEE was pulsed with 100 kHz calibration pulses — > we expect t0 decision in every 10 us
- The time interval between adjacent trigger decisions are estimated and they are consistent with the calibration pulses

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∽ hi t_cnt	137	137	1	0
∽ t0_1	1362	1362	13626 Х	17001
∽ t0_2	1021	1021	10217 X	13626
∽ t0_3	6841	6841	6841 X	10217
		4 >		
Waveform captured	Jun 1	8, 201	17 2:59:40 PM	X: -50 • 0: -50 • Δ(X-0): 0

• Photon Flux significantly above desired levels

Beam Background

- 8 MHz/PMT
- 2 64 MHz/Board Stack
- 3 256 MHz/TOP Bar



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t0s in presence of Background (electronic noise)

Bus/Signal	х	0	100	-90	-80	-76	-61		50 	-40	- 30		20	-10		10		20	30 	40	50	60	70	8	0 	90 	100	110	120	130	140	150
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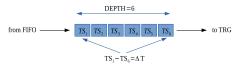
- Triggers are too frequent in presence of background since every timestamp arrive at UT3 are processed
- This problem is already known from a software simulation
- Possible solution: Run Trigger algorithm only during the arrival of timestamps belong to a signal

Image: A matrix

- Initially, TSs go to "Shift register" and continuously monitored by "Data redirection" (path 1)
- O whenever $\Delta T < \text{THRESHOLD}$
 - i Stop taking TSs from FIFO
 - ii Recover the 6 TS which is already in Shift reg.

(path 2& 4)

 Continue to take TSs from FIFO, after recovering 6 TS in shift reg. (path 3& 4)



- FIFO shift register enable Data redirection. Trigger FSM
- Signal identification efficiency should be maximized by optimizing THRESHOLD and DEPTH

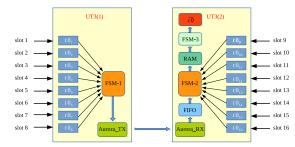
Firmware with IHTD

- shiftreg_cnt
- shiftreg_full
- \bullet deltat_threshold_flag
- shiftreg_recovery_flag

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$$\tilde{t0} = \frac{\left(\sum_{i=1}^{i=16} t0_i L_i\right)}{\left(\sum_{i=1}^{i=16} L_i\right)}$$

- t0₁-t0₈ on UT3(1) and t0₉-t0₁₆ on UT3(2)
- All t0s on UT3(1) are send to UT3(2) (4-lane AURORA with each lane is 5.08 Gbps)
- All t0s are temporarily stored on a RAM until t0 is estimated



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Combined t0 on UT3(2)

sun_logL 0		500 -460 -420 -380 -340 -300 -260 -220 -180 -140 -100 -60	-20 20	60 100 140 18		460 50
	0000 0000	000000063054232		X	00000005DE34F01	
sun_t0°logi	0000 0000:	000018E0276C0669		X	0000123F706DD782	
nean_t0	0000 0000	000000000004811000000019749117		X	0000000000031C1000000025F016F1	
counter	64 39	0)	X.	0	
state_combine	1 1	0	X 1	X	0	
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RAM<2>	0000 0000	00000000		X	00000000	
RAM<3>	0000 0000	00000000		XX	00000000	
RAM<4>	0000 0000	00000000		XX	00000000	
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Combined t0 on UT3(2)

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- sun_t0°logi	0000	0000	000018E0276C0669				X	X 0000123F706DD782
- nean_t0	0000	0000	00000000004811000000019749117					X 000000000031C1000000025F016F1
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- RAM<2>	0000	0000	0000000					00000000
- RAM<3>	0000	0000	00000000					00000000
- RAM<4>	0000	0000	00000000					00000000
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- RAM<8>	0000	0000	00000000					00000000
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Combined t0 on UT3(2) (latency added)

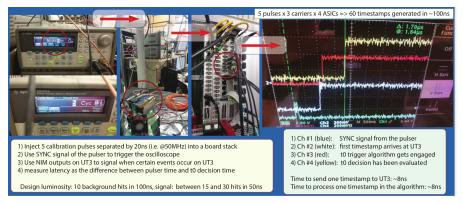
Bus/Signal	x	0	500 -460 -420 -380 -340 -300 -260 -220 -180 -140 -100	-60 -20 20 60 100	140 180 220 260 300 340 380 420 460 5
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► RAM<4>	00000905	00000000	00000000	XX	00000000
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- RAM<6>	00000903	00000000	00000000	X0000 X	00000000
- RAM<7>	00000905	00000000	00000000	X X	00000000
- RAM<8>	00000902	00000000	00000000	XX	00000000
- RAM<9>	00000902	00000000	00000000	XX	00000000
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- RAM<16>	00000905	00000000	00000000	XX	00000000
reset_RAM	0	0			
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- t0_Contoller	BC1CBC1C	BC1CBC1C			
- Bar_number	E	E	E	X E XXX	E
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Latency



- Latency estimated for single Bar by injecting calibration pulses in to FEE
- Latency depends on number of hits and have contribution from AURORA, XILINX cores used for weighted sum of t0 etc.
- Overall expected latency below 2.5 us

- $\bullet\,$ Timestamping is implemented in all latest FEE FW and reliably transmitting them to UT3 at 5.08 Gbps
- The algorithms for collecting and combining t0 decisions from individual bars have been designed and tested at KEK
- TOP Trigger latency is measured and the value is well within maximum allowed limit
- TOP Trigger FW with Instantaneous Hit Time Density (IHTD) is designed and tested at Pittsburgh. Working on optimization of various parameters to get best possible performance of Trigger FW.
- Soon start working on interface to GDL.