Readout Upgrade: Schedule and Guideline

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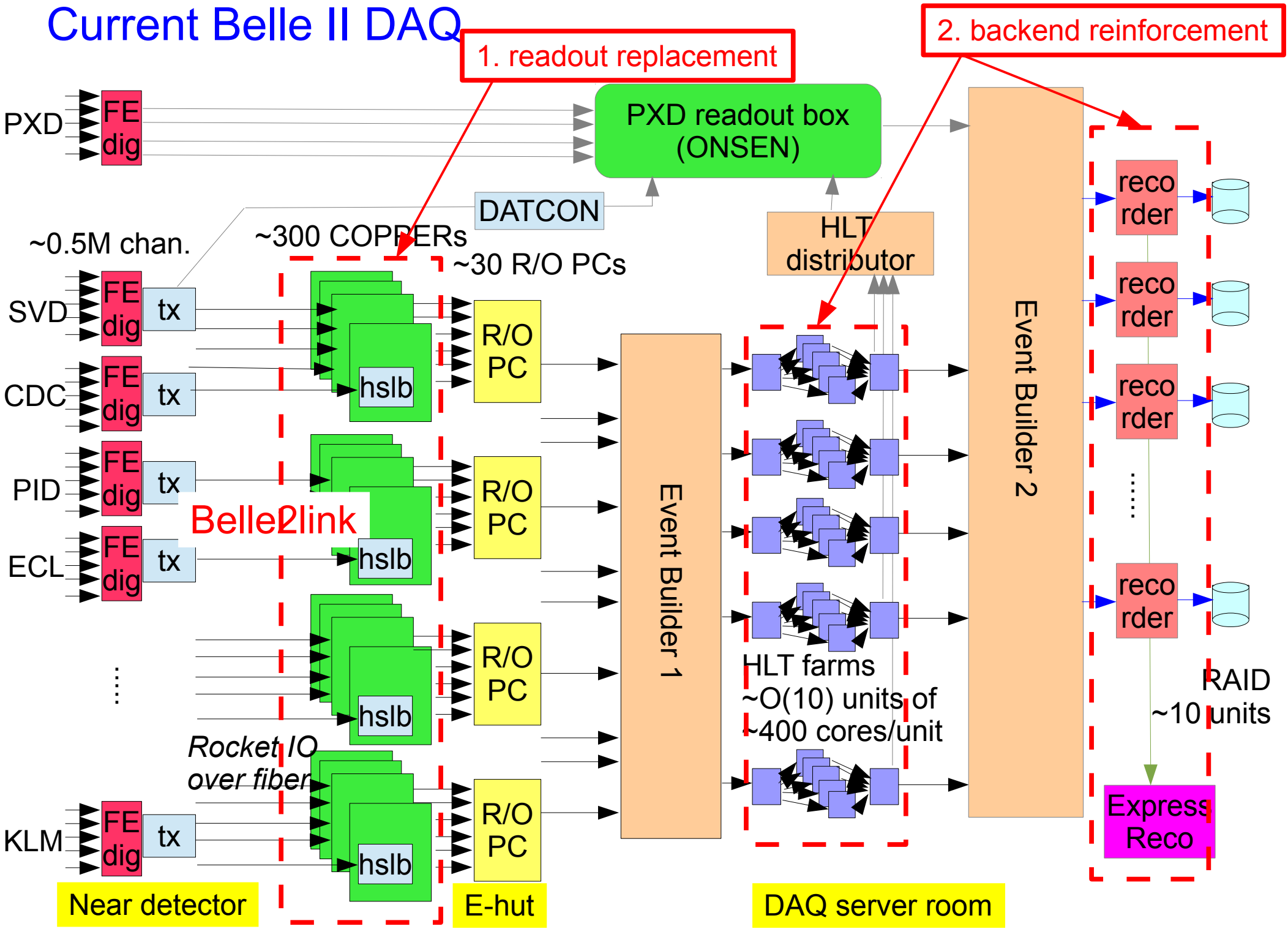
Readout Upgrade

- COPPERs are already obsolete and we agreed to start R&D on the new readout system last year.

- In the DAQ meeting in March, it was decided to keep the current implementation schedule unchanged although Belle II commissioning was deferred:
  * Start prototyping in late JFY2018 and two years for R&D.
  * Start mass-production in JFY2020 and three years for prod.
  * Start replacement of COPPERs from JFY2021 and complete replacement by the end of JFY2023.

- To keep up with the schedule, we need to fix the prototype design by Oct.2018.

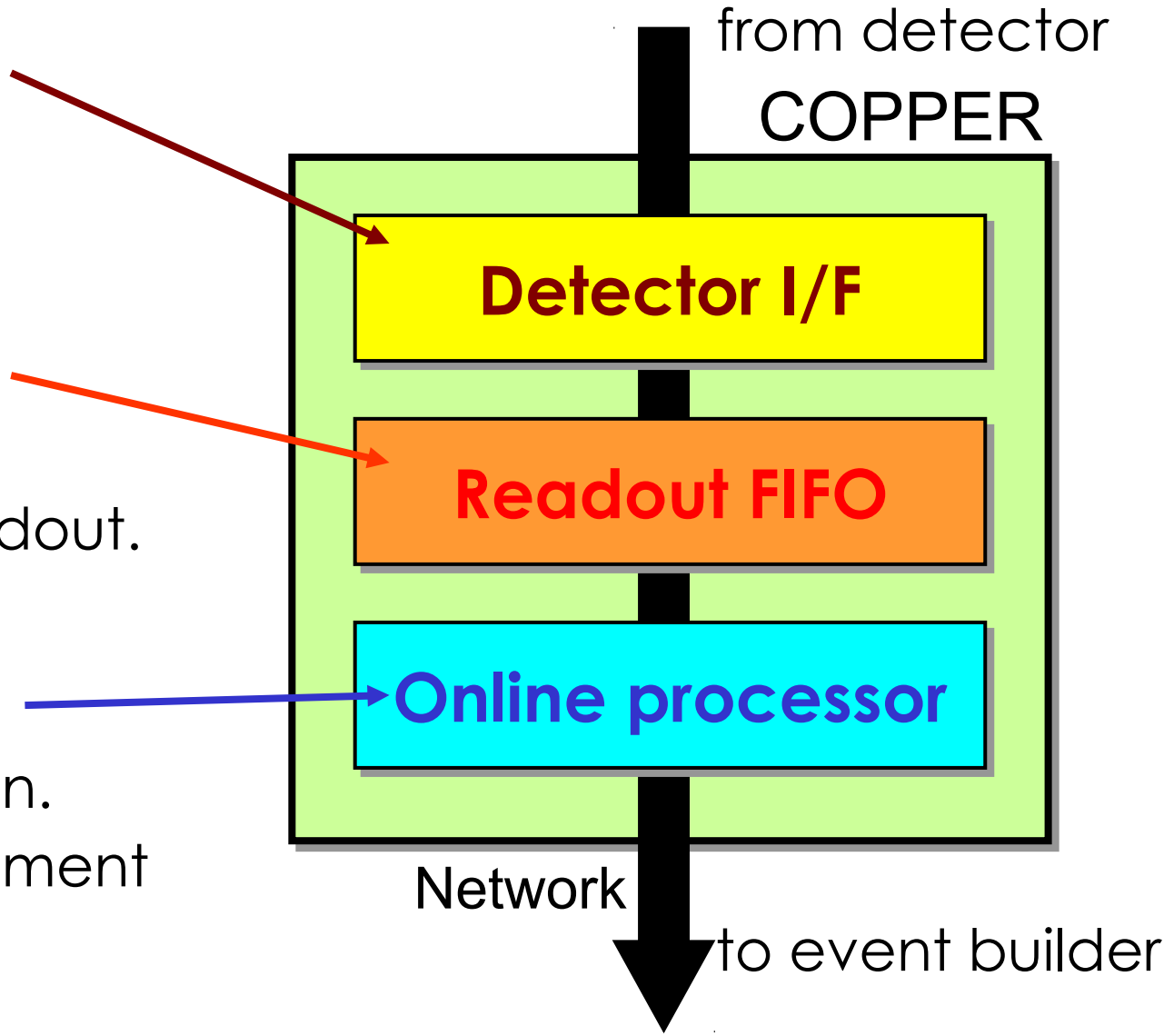

Current Belle II DAQ
1. readout replacement
2. backend reinforcement
PXD
FE dig
PXD readout box (ONSEN)
DATCON
HLT distributor
~0.5M chan.
~300 COPPERs
~30 R/O PCs
SVD
CDC
PID
ECL
KLM
tx
hslb
R/O PC
Belle2link
Rocket IO over fiber
Event Builder 1
Event Builder 2
HLT farms
~O(10) units of
~400 cores/unit
reco rder
RAID
~10 units
Express Reco
Near detector
E-hut
DAQ server room

What is COPPER?

COPPER is a unified “pipeline read-out platform” module.

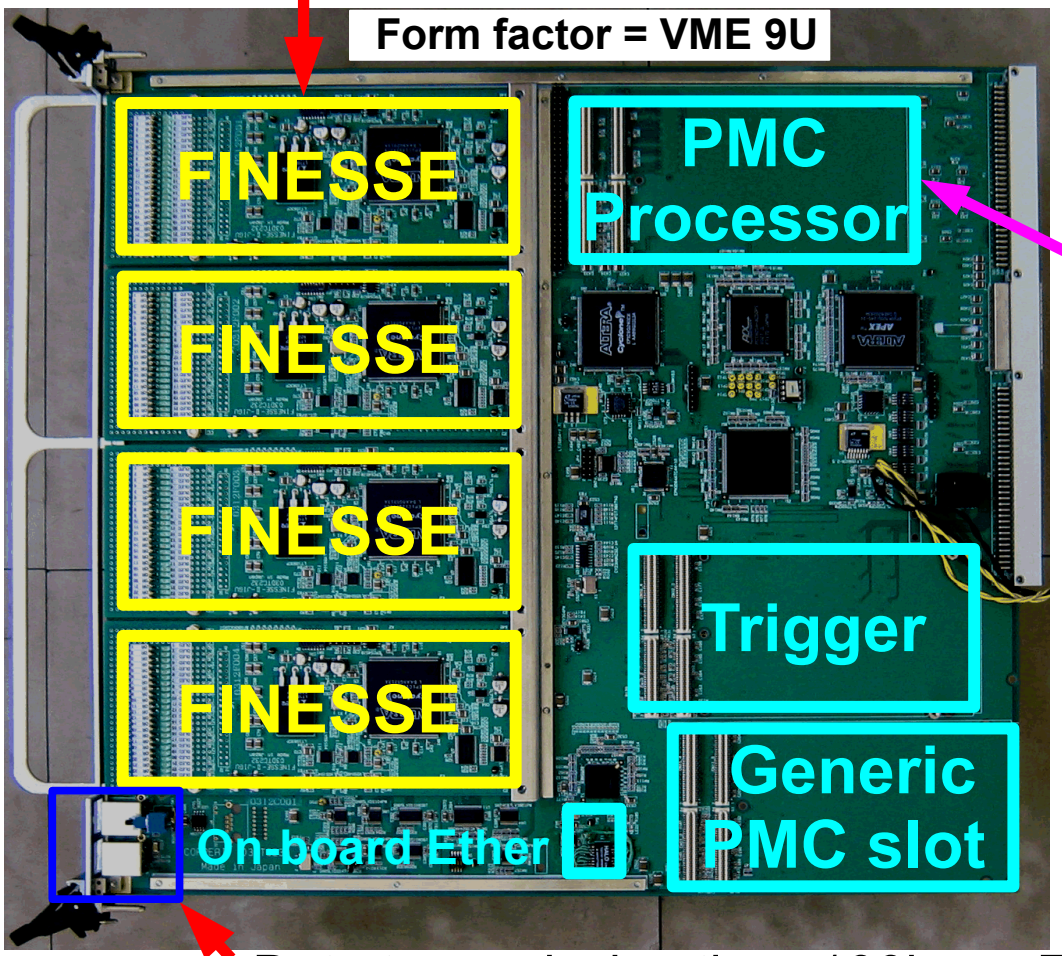
(Common Pipelined Platform for Electronics Readout)

- Detector I/F
  - Signal digitization.
  - L1 pipeline.
- Readout FIFO
  - Event buffers for asynchronous readout.
- Online processor
  - Data size reduction.
  - Data link management to event builder.
  - Linux operated



COPPER : Reality

digitizers are mounted as daughter cards



CPU card (Linux)

Radisys: EPC-6315
(Pen3@800MHz)
GE-FANUC: PSL-09
(PenM@1.4GHz)

Densan: ATOM@1.6GHz
for Belle II

Data transmission thru. 100base-T -> 1000Base-T (COPPER III)

For Belle II DAQ, “HSLB”, which is a high-speed optical link receiver, is mounted as “FINESSE”.

COPPER History

- Early 2002
  - Design from scratch.
- Mid. 2003
  - COPPER prototype.
- Mid. 2004
  - Upgrade to COPPER-II.
  - More than 30 kHz L1 rate for > 400 bytes/ev/FINESSE.
- Early 2005
  - # of FINESSE variations increased eventually.
- Mid. 2005
  - Installation to the Belle EFC.
- 2006-
  - Belle DAQ Upgrade
  - Telescope array DAQ
  - KEK TRIAC DAQ
  - J-PARC beam line monitor
- 2008-
  - Belle II DAQ design with COPPER
- 2009
  - Upgrade to COPPER-III
- 2010-
  - Belle2link development
- 2014-
  - Belle II DAQ operation started!

Why COPPERs in Belle II DAQ?

* We had accumulated a lot of experience with it in the previous Belle experiment.
  <- Belle DAQ upgrade from FASTBUS TDC to COPPER TDC.
  => Stable DAQ operation from the beginning of Belle II.
* Cost reduction by recycling Belle COPPERs.
  => 1/3 of COPPERs are recycled from Belle.

- However, it turned out to be difficult to maintain the system until the very end of Belle II experiment, which is supposed to run over 10 years.

Why is the maintenance of COPPER system difficult?

1. The design of COPPER is based on the old PC technology, such as PCI-bus, which is already obsolete.

2. The production of many components used in COPPER is already discontinued.
   * Network controller chip
   * Chipset used in the CPU card (PrPMC)
   * Various control chips used in COPPER (FIFO.....)
   .....

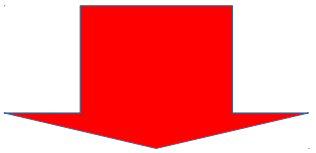
3. The production company of COPPER says they cannot support COPPERs any more.
   - *We still have a number of backup COPPER modules, but it is limited (especially COPPER III, majority of COPPERs in our DAQ).*

4. Cannot keep up with the evolution of Belle II software.
   * COPPER CPU has the 32bit architecture, but recent Belle II software, which is heavily utilized in COPPER CPU, is now all 64bit based while abandoning the support for 32bit.....

Further concern:

- There could be a chance that the accelerator luminosity goes up beyond the design value.
  <- Remember the fact that KEKB achieved twice luminosity of the design value!

- In this case, the processing power of COPPER becomes the bottleneck of DAQ, which was designed for the luminosity up to $L=8x10^{35}$
  * PCI bus speed cannot manage the expected data flow.
  * Lack of processing power of CPU card.



Replacement of old COPPERs is required.

Strategy

Replace COPPERs with a number of high-density FPGA based processing cards equipped in xTCA crates without modifying other components.

- We will keep the same detector front-end and the data transport through Belle2link.
  -> No change in the detector interface.

- We will keep the same backend readout (readout PC, event builder, HLT.....).
  * Ethernet(GbE) based connection

Timeline

- Start the R&D for the upgrade from late JFY2018.

- It will require two years to complete the R&D.

- We will start the mass production of new readout cards from next year after the R&D, and complete the production in 3 years.

- The actual replacement of COPPERs will start in the 2nd year of the production at the earliest.

- Subsystem-by-subsystem replacement is planned (as we did in Belle I to replace FASTBUS TDC with COPPERs).

- Complete the replacement by JFY2023 at the earliest.

Cost Estimation

- Cost estimation given to Belle II Financial Board in 2015 assuming the start of R&D in 2018.
- Cost was estimated based on Yamada-san's proposal

a) Preparation cost

* Two years for preparation
* Development of prototype card
* Firmware development
  <- we can make use of existing development tools.

(Unit: 1,000yen)

FY2018		FY2019	
Budget		**Budget**	
Prototype board	3,000	Prototype board	4,000
MCH board	400		
uTCA shelf	600		
Total	4,000	Total	4,000
Plan		**Plan**	
• Design and production of a prototype board • Development of firmware		• Debugging with prototype boards • Designing of the mass production board • Development of firmware	

b) Production cost

* Start board mass production from FY2020
* Complete production in FY2022 to install all by FY2023.

(Unit: 1,000yen)

FY2020		FY2021		FY2022	
Budget		**Budget**		**Budget**	
Board production	1,400x18 =25,200	Board production	1,400x24 = 33,600	Board production	1,400x24 =33,600
Cable, patch panel for installation	500	Cable, patch panel for installation	500	Cable, patch panel for installation	500
MCH boards	400x6 =2,400				
uTCA shelves	600x7 =4,200				
Total	32,300	Total	34,100	Total	34,100
Plan		**Plan**		**Plan**	
➢ Mass production (SVD, TRG, TOP and ARICH) ➢ Test of boards ➢ Installation work ➢ Firmware development, debugging		➢ Mass production (CDC and ECL) ➢ Test of boards ➢ Installation work ➢ Firmware development, debugging		➢ Mass production (KLM and 10 spares) ➢ Test of boards ➢ Installation work ➢ Firmware development, debugging	

We will keep FTSW/Belle2link unchanged as the detector I/F.
The DAQ backend (event builder sw, HLT....) is also unchanged.

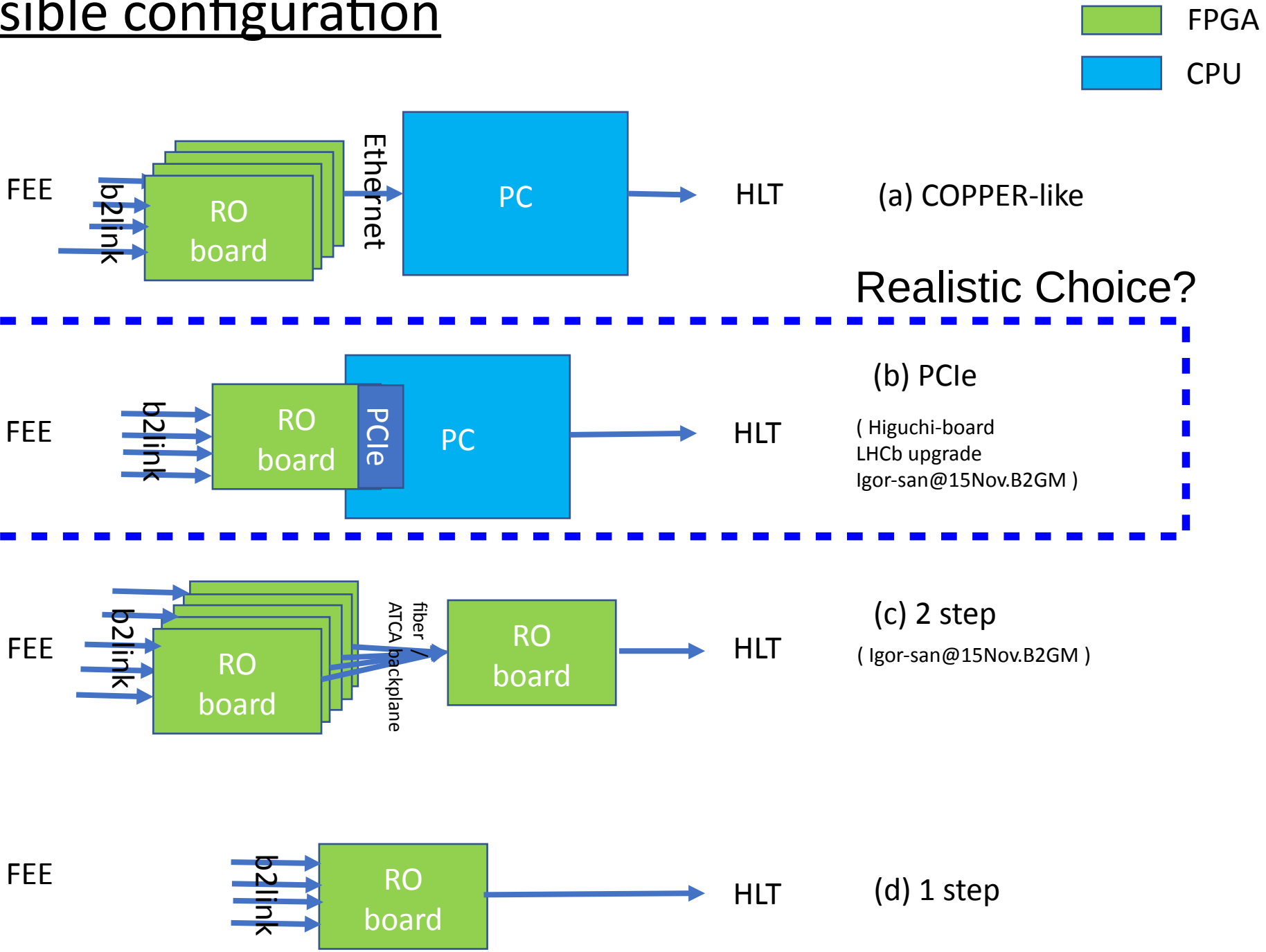
- Hardware is not a main issue of R&D. It can be an existing or commodity hardware consisting of multiple optical I/Fs, a large FPGA, and either a PCIe or a GbE/10GbE output.

The main R&D goal is the firmware.
* Revisiting Belle2link receiver core. -> Need Zhen'An's help again.
* Porting COPPER processing which is done by software to FPGA processing. -> most difficult part.
* Interface with existing/commercial transmission core (PCIe/10GbE).

- But at the time of module production, the FPGA should be the latest one, and some R&D on hardware is also required.
(But anyway, the target FPGA is restricted to Xilinx's so that we can recycle our previous developments.)

Possible configuration

S.Yamada



- We will start R&D utilizing the existing hardware
  * TUM card originally developed for COMPASS
  * PXD R/O card originally developed as a backup
  * Commercial FPGA evaluation card (for new FPGA evaluation).

- We will discuss the further detail in
  * TRG/DAQ workshop in Taipei in August.
  * A workshop focused on the upgrade in Sep. or Oct.
    => Could be attached to next B2GM, decided soon (Oct.16-17?)

- Everyone interested in the upgrade project is welcome.
  In particular, firmware specialists!

Example of task sharing (discussion item)

1. Detector interface : Belle2link (and FTSW?)
   * Need to implement HSLB firmware in new readout card
   * Revisit to sender firmware might also be necessary
   * Update in FTSW related firmware together?
   * High-density implementation (>20 optical inputs/board)

2. Porting of COPPER data processing software in FPGA firm
   * Data formatting
   * Event building
   * Data reduction

3. Output implementation
   * Possibly PCI-e interface to be connected to readout PC
   * Option : direct 10GbE output with some ethernet core.
   * Readout PC software is a part of coverage.

4. Hardware development for board mass-production
   * Evalulation of latest FPGA
   * High-density implementation of optical fiber receiver
   * PCI-e interface

- For the task sharing, we need to have a clear interface definition between firmware blocks on the agreed hardware configuration.

- Decision of who will do what -> By next workshop scheduled in Oct.
  * The workshop date is tentatively set on Oct. 16-17 (at KEK).
    -> but could be shifted a day or so to avoid conflict with BPAC.