DAQ Development at TUM

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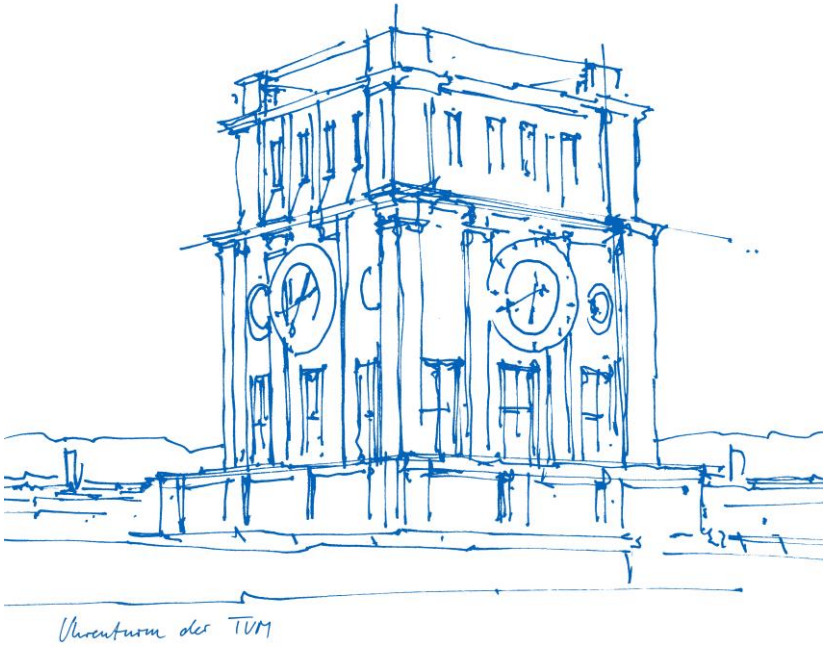
Taipei



Talk Overview

- IFDAQ
- IFDAQ in COMPASS experiment
- New developments
  - Crosspoint Switch
  - Kintex DAQ module

IFDAQ

Intelligent FPGA-based DAQ

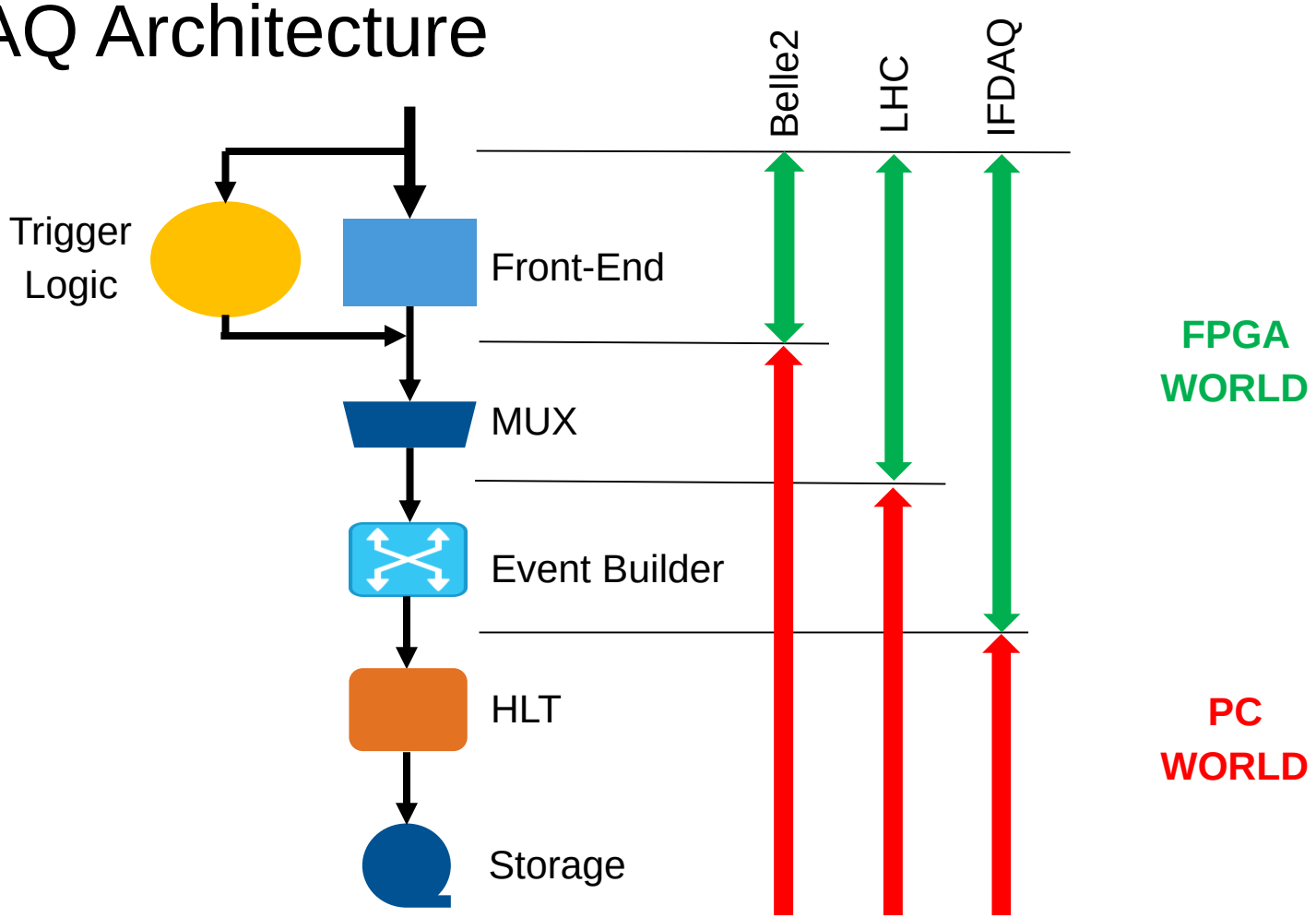
Motivation :

- Develop reliable and high performance DAQ
- CPU vs FPGA (Sequential vs Parallel)
  - Performance of sequential execution strongly depends on algorithm complexity
  - In CPU Recovery of hanging process takes significant time
- Only FPGA allows to build real real-time systems
- Limits number of real time processes or completely exclude them
- Intelligence : FPGA takes full responsibility for reliable data transmission from FEEs to PC
  - Data flow control to provide synchronization of data streams
  - Event building
  - **Error diagnostic and error handling to prevent DAQ crash**
  - Automatic resynchronization of FEEs with the rest of the system

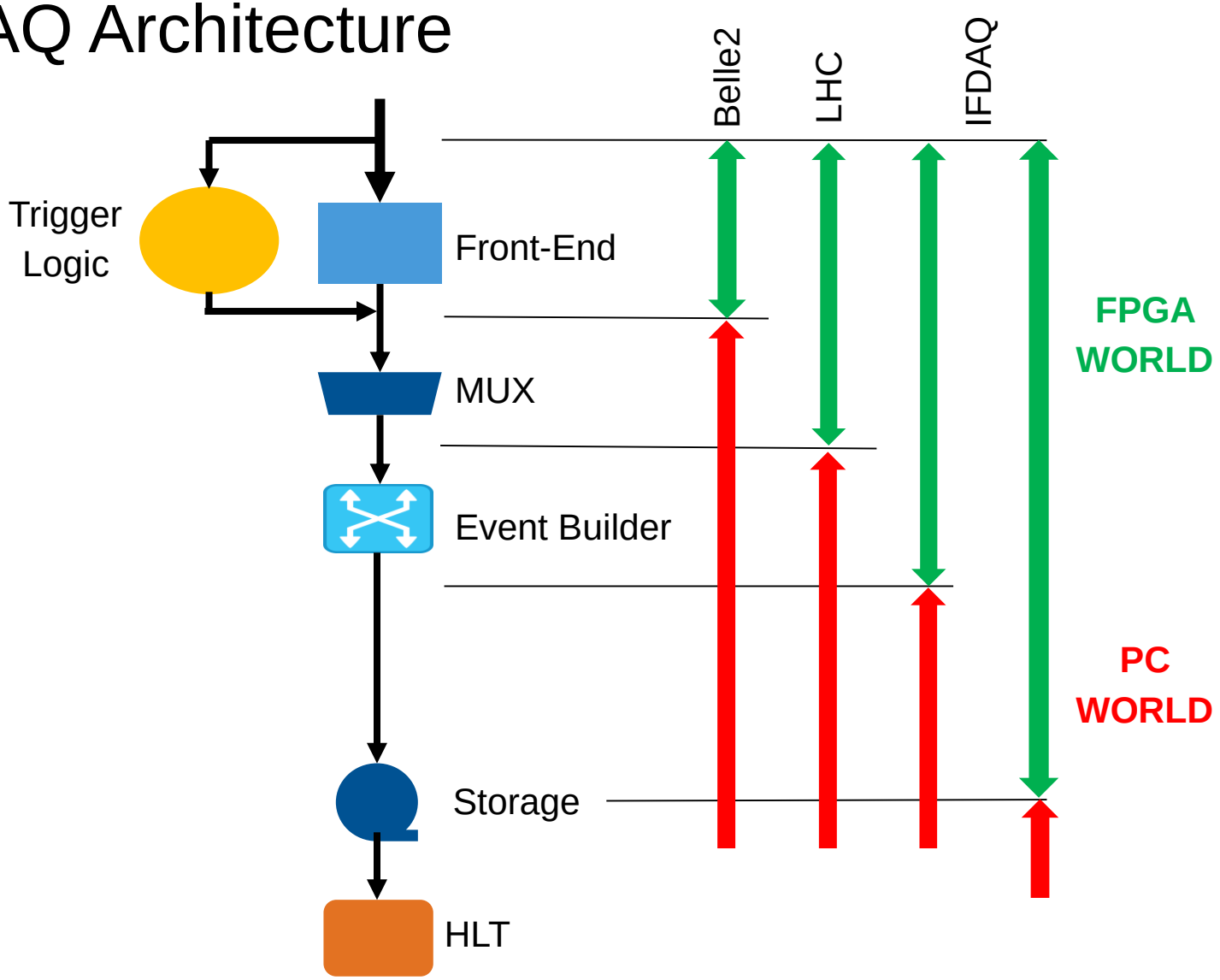
    FEEs can be attached to DAQ at any time

    Continuous data taking mode of operation => 100% uptime
- System redundancy & hardware failure diagnostic for automatic exclusion failed hardware

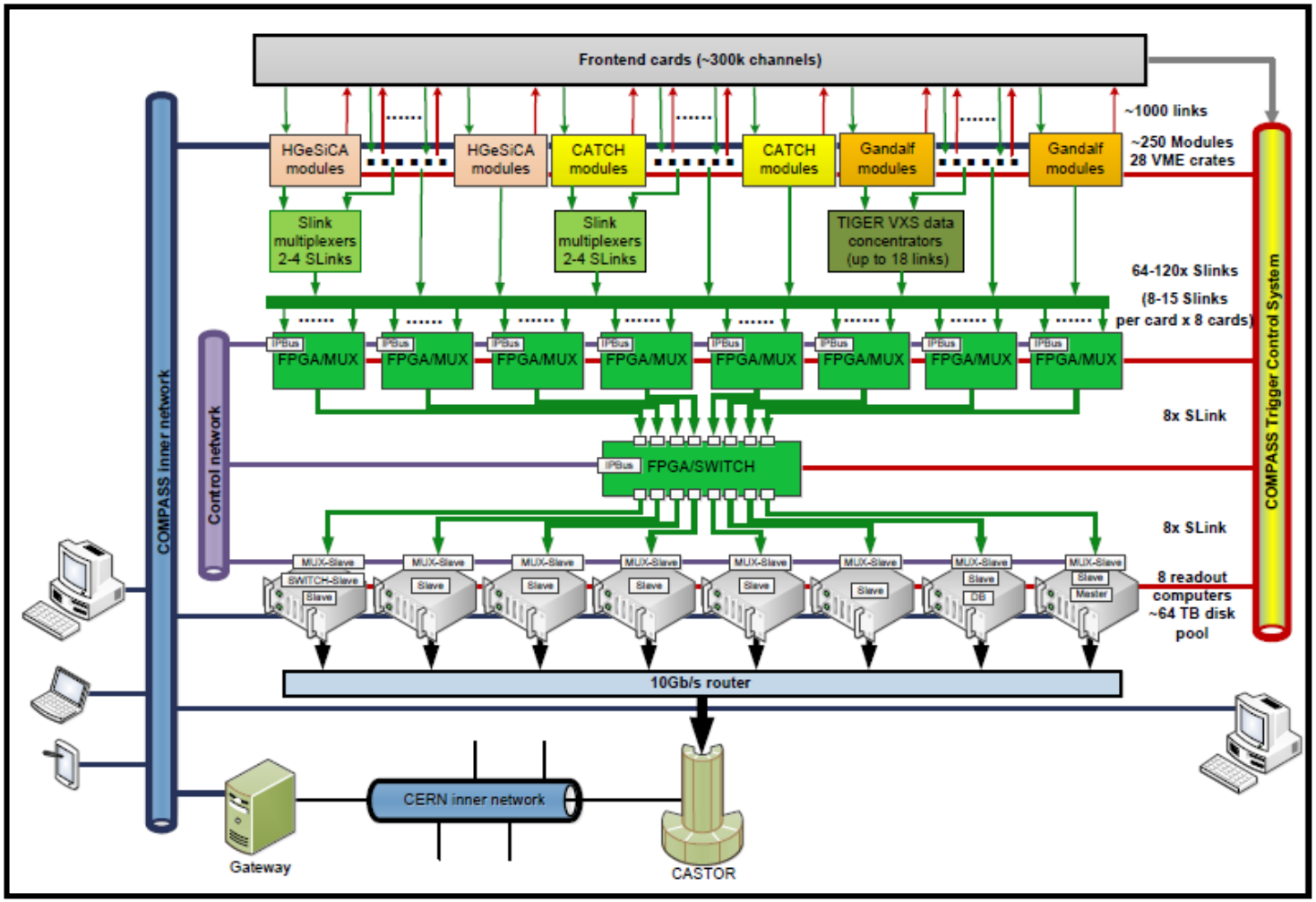
DAQ Architecture



DAQ Architecture



COMPASS DAQ

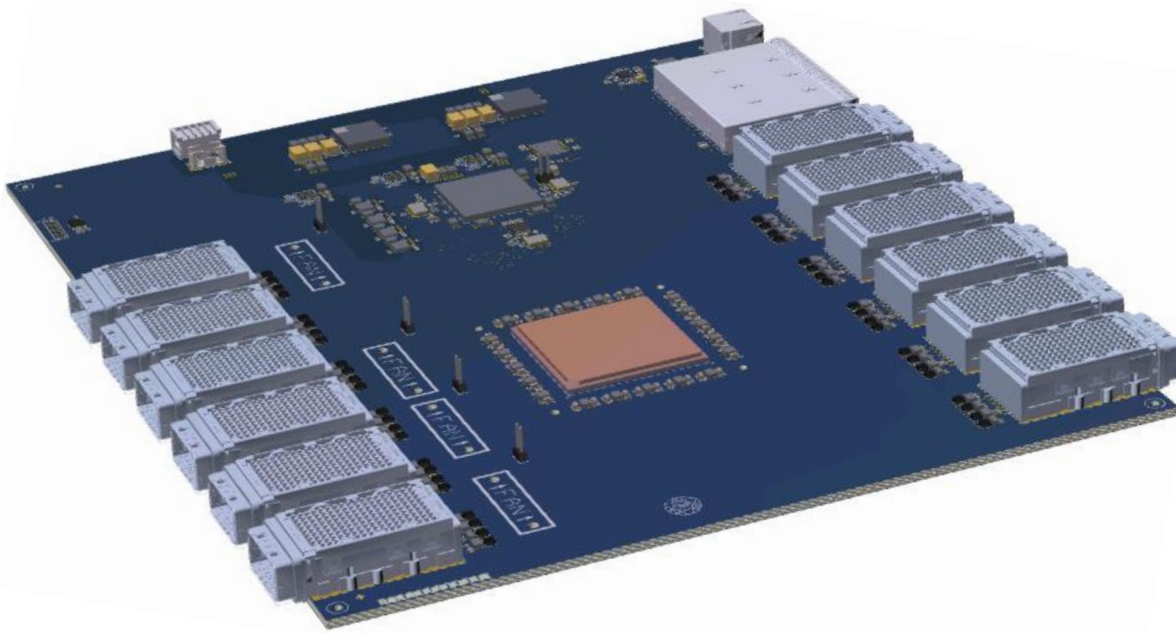

Frontend cards (~300k channels)
~1000 links
HGeSiCA modules
HGeSiCA modules
CATCH modules
CATCH modules
Gandalf modules
Gandalf modules
~250 Modules
28 VME crates
Slink multiplexers 2-4 SLinks
Slink multiplexers 2-4 SLinks
TIGER VXS data concentrators (up to 18 links)
64-120x Slinks
(8-15 Slinks per card x 8 cards)
IPBus
FPGA/MUX
8x SLink
FPGA/SWITCH
8x SLink
MUX-Slave
SWITCH-Slave
Slave
Master
8 readout computers
~64 TB disk pool
10Gb/s router
COMPASS inner network
Control network
COMPASS Trigger Control System
CERN inner network
Gateway
CASTOR

CROSSPOINT-SWITCH

Crosspoint Switch – Hardware Design

Crosspoint Switch Components

- **interfaces:**
  - 12 x 12 channel CXP transceiver (MPO fiber connectors)
  - Ethernet for IPbus
  - JTAG
  - TCS (Trigger Control System) receiver
- **Switching and Control:**
  - **Vitesse VSC3144-02** – fully configurable, asynchronous, 6.5 Gbps crosspoint switch
  - **Xilinx Artix-7 FPGA** for switch control and monitoring



- **Interface FPGA – Crosswitch:**
  - 90 MHz, 11-bit parallel data bus
  - Multiple program assignments can be queued and issued simultaneously ⇒ fast programming

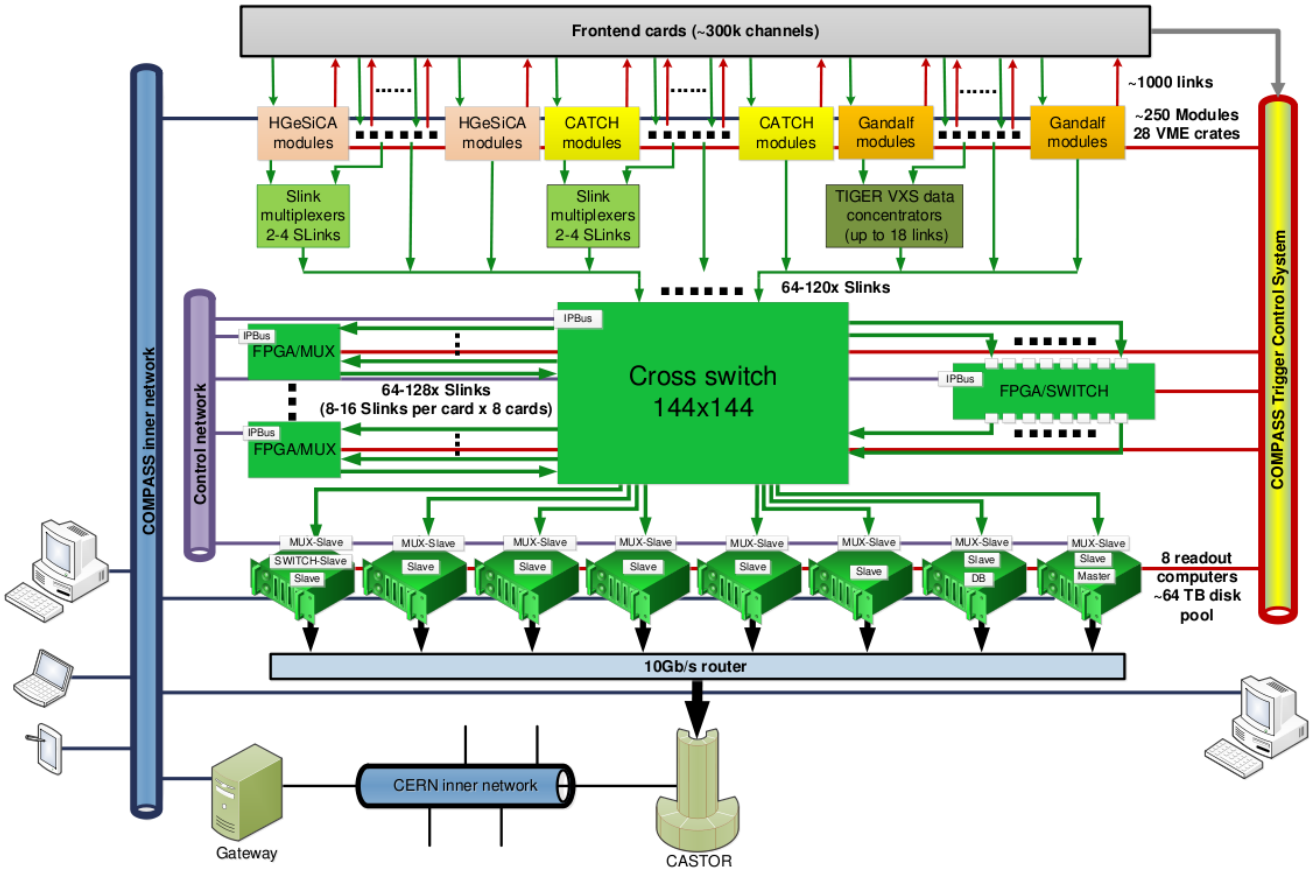
Status: module in production

Crosspoint Switch Integration

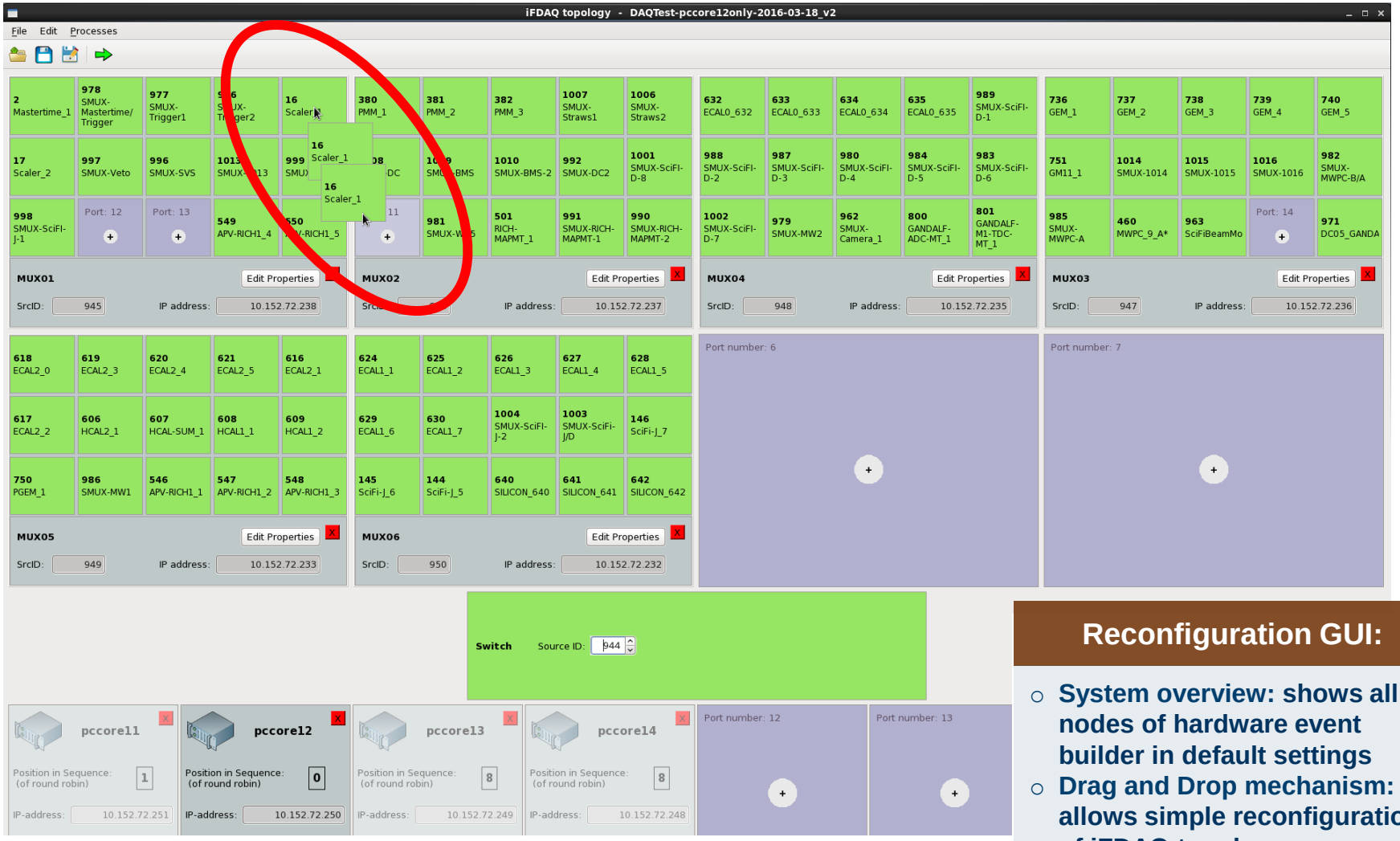
Crosspoint Switch

- connects:
  - FE electronics
  - DHCmx modules
  - DHCsw module
  - DHCsb modules
- purpose:
  - Ease of load balancing
  - System redundancy to compensate hardware failures

⇒ provides fully customizable network topology



Crosspoint Switch - Software



Reconfiguration GUI:

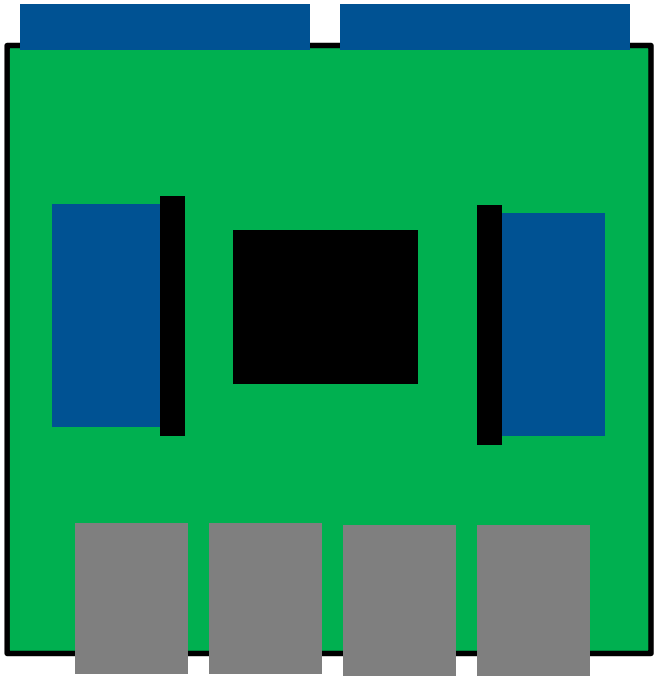
- **System overview: shows all nodes of hardware event builder in default settings**
- **Drag and Drop mechanism: allows simple reconfiguration of iFDAQ topology**

Kintex Ultra Scale DAQ Module

Development of Kintex UltraScale DAQ Module

Technical parameters :

- XCKU095-A1156
  - 1.2 M logic cells
  - 60 Mbit Block RAM
  - 64 x 16Gb/s
- 2 x 16 GB DDR4 SODIMM, combined data throughput 10 GB/s
- AMC connector Interfaces
  - B2TT/TCS
  - Ethernet(IPBUS)
  - 15 x 16Gb/s
- Front panel interfaces
  - 48 x 16Gb/s



THANK YOU