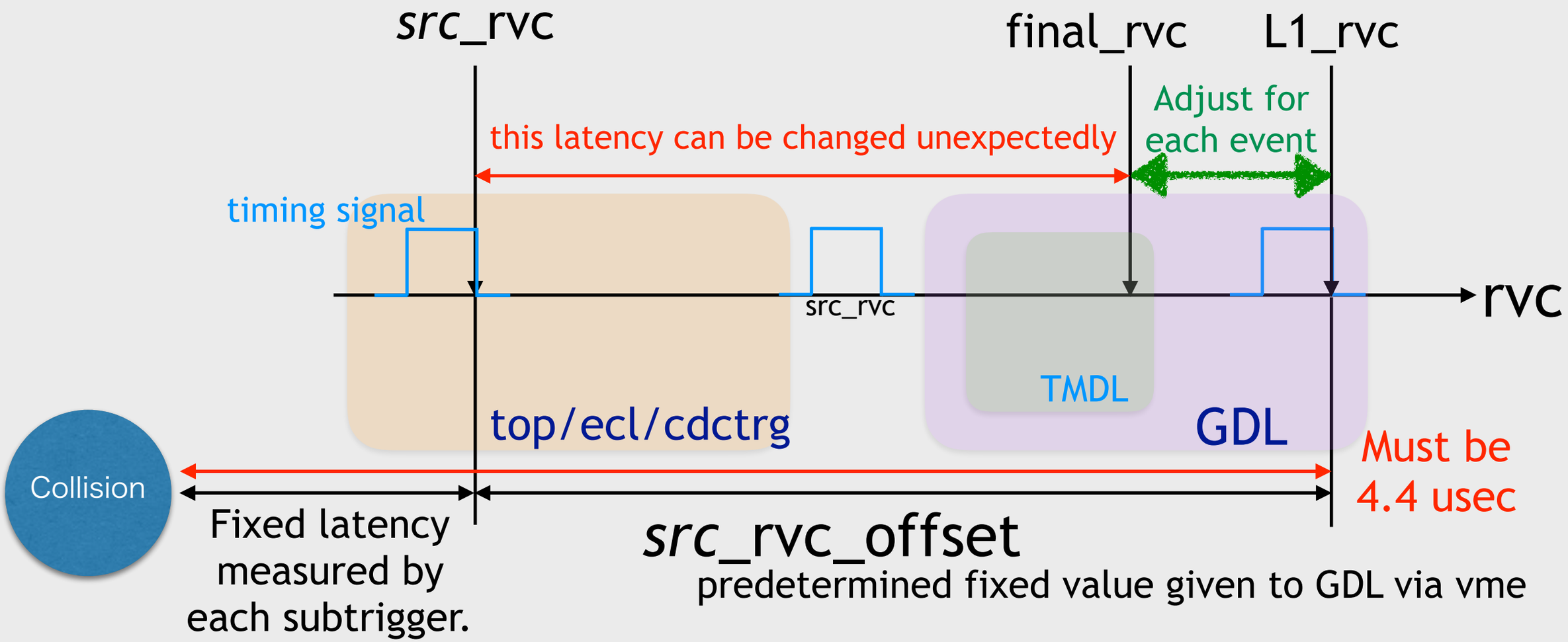
GDL Status

TRG/DAQ workshop@NTU
20170823
H. Nakazawa (NTU)

Contents

- Timing Shift Problem
- Random trigger
- Plans for Slow Control

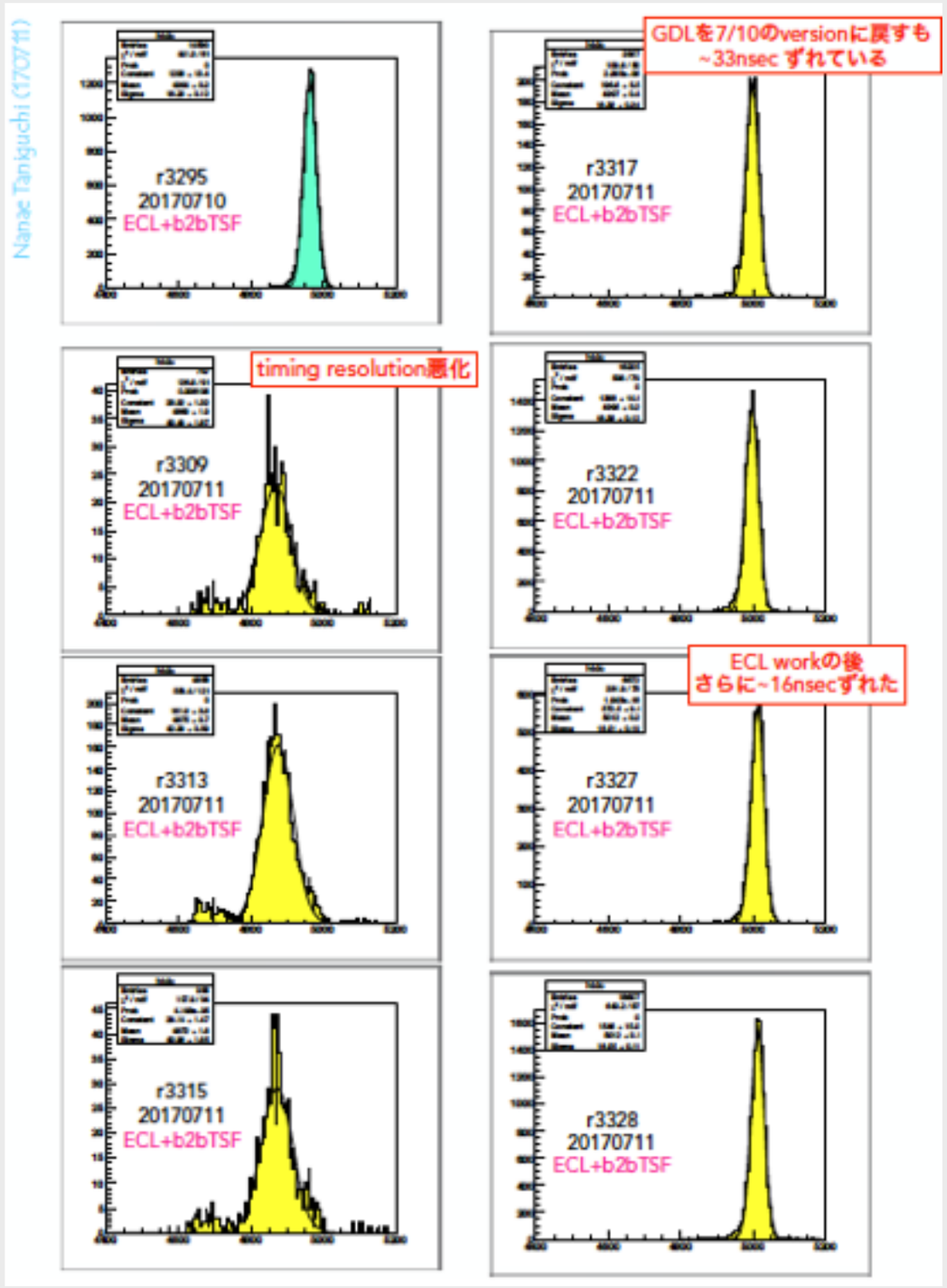
Timing Adjustment using rvc (revolution clock)



⟷ = src_rvc + src_rvc_offset - final_rvc

Timing Shift Problem

- Timing Shift observed after
  - GDL firmware update
  - ECL work
  - Shutdown
- Checked with CDC fastest hit



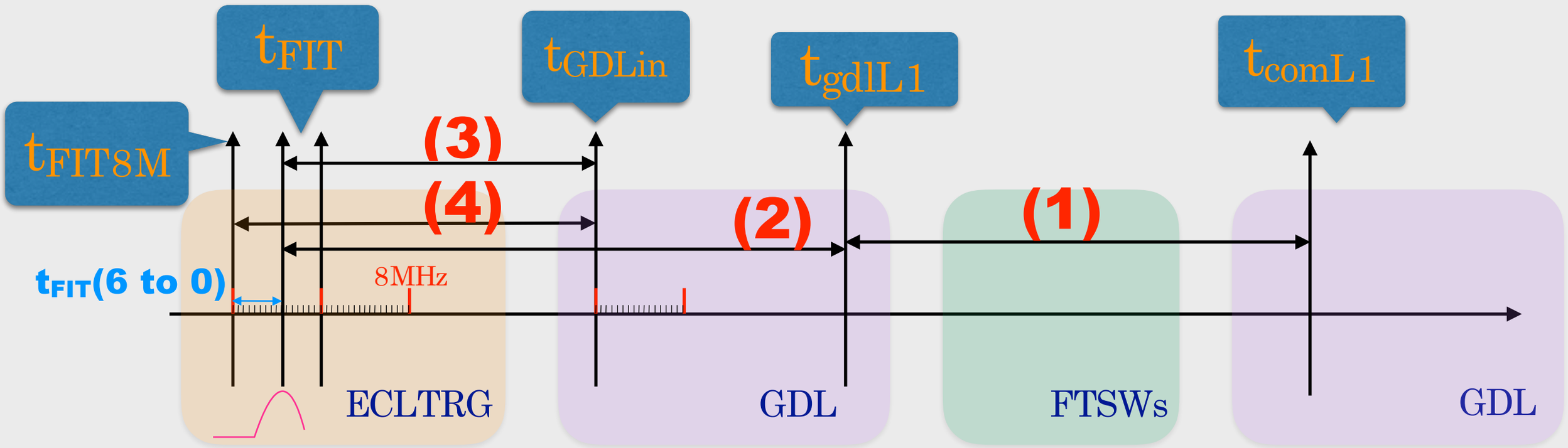
GDL Timing Monitor

(1) Latency between GDL L1 and common L1
Must be at reference value

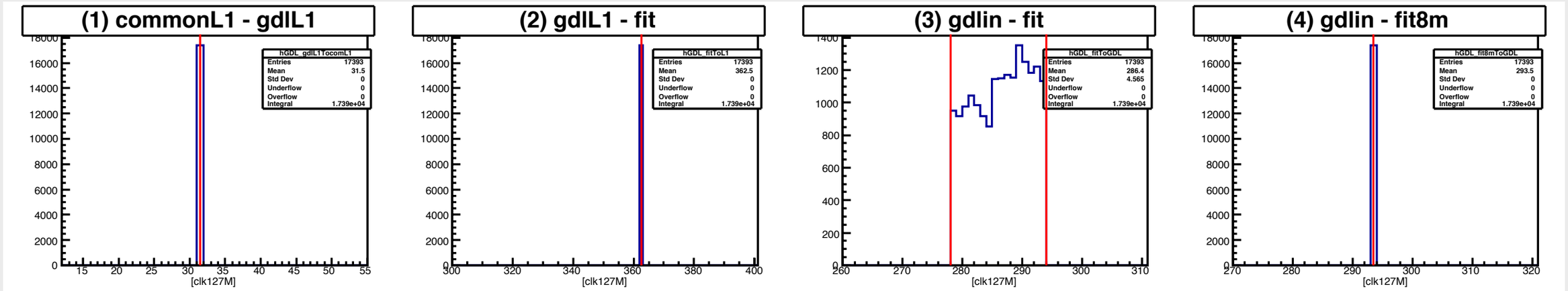
(2) Latency between ECL timing and common L1
Must be at reference value

(3) Latency between ECL timing and GDL in
Must be within reference range

(4) Latency between ECL timing (8 MHz clock) and GDL in
Must be at reference value

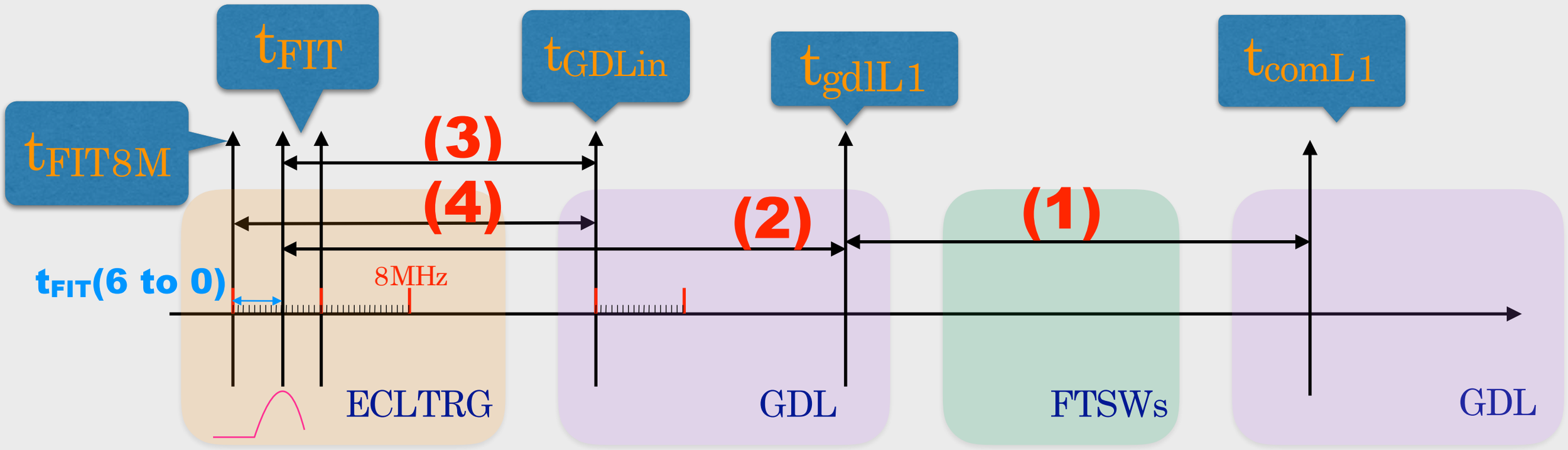


GDL Timing Monitor



r3964 (Last night)
r3845 (early run in Aug. GCRT)

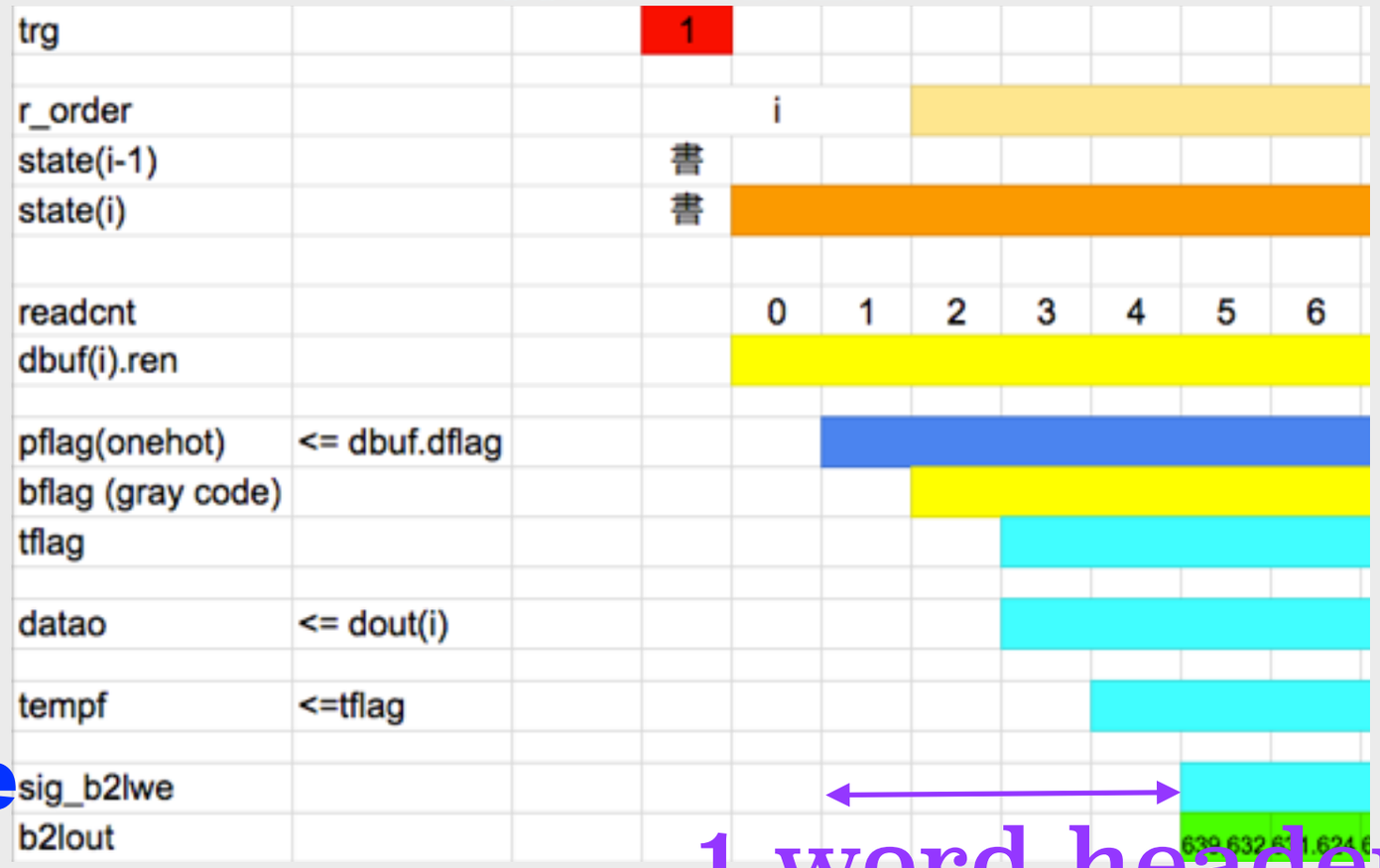
- No timing shift in August runs
- Unpacker and HistoModule ready (feature/gdldqm)
- Will be added to DQM



"Header" added to b2l readout

- To record revoclk of common L1
- Will be extended to record config parameters

common L1



b2lwe

1 word header
for comL1_rvc

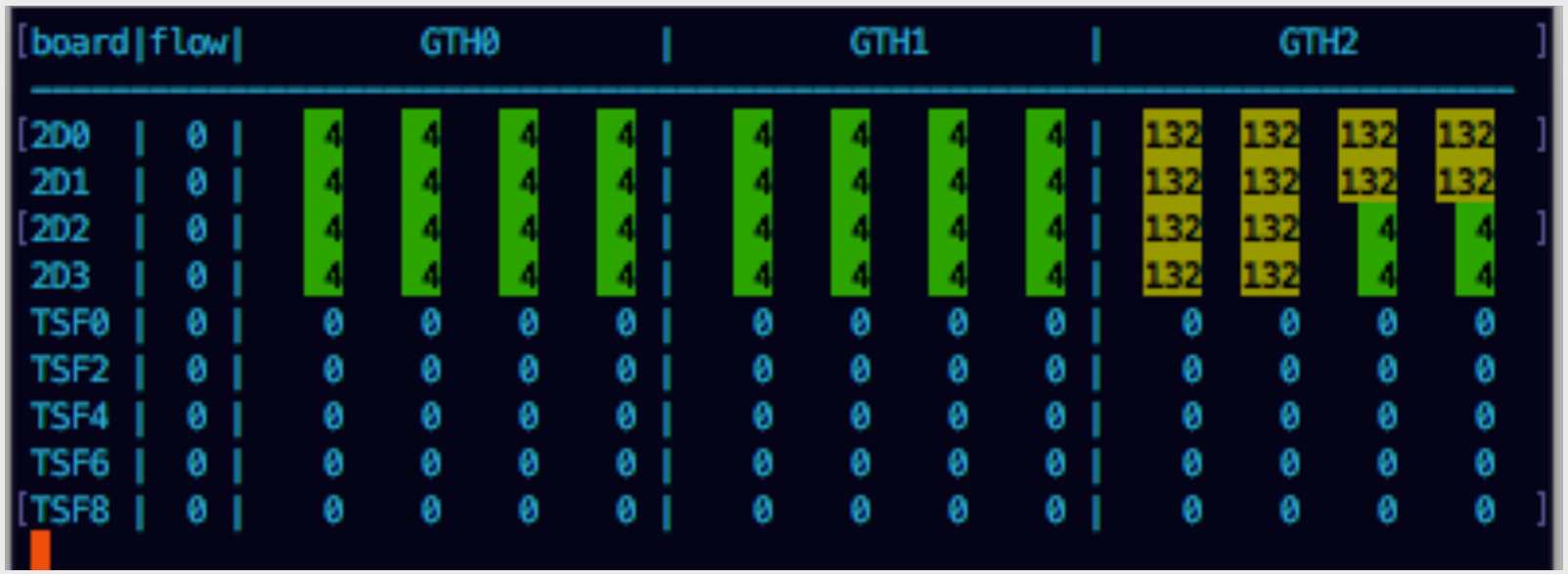
Random Trigger

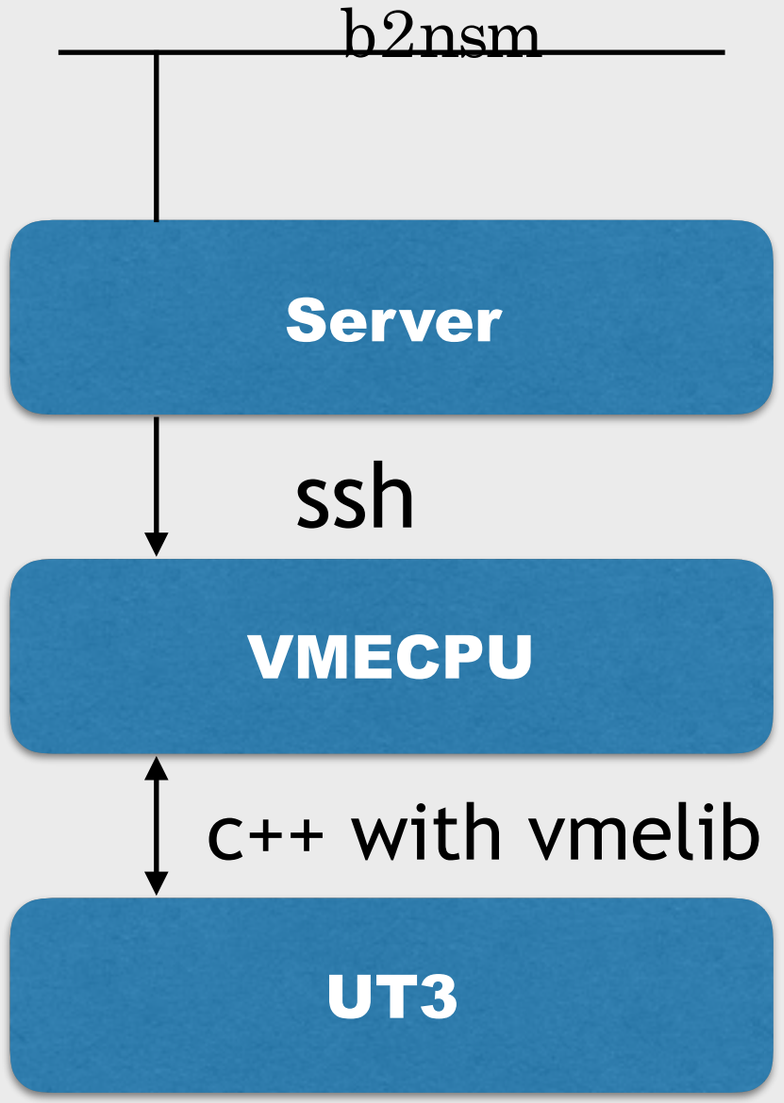
- Included in original design.
  - Background data without collision
  - Bhabha-based random trigger planned
- Random Flag to all PSNM bits
  - Changeable via VME
- Self Timing, TimingType=RANDOM
- Recently requested by CDC group
  - (ECL_timing && tsfSingle) || Random(1Hz)
- A new input and ftd bit, period <= periodin;
  - periodical 1 MHz (properly prescaled).
- Worked as expected.
  - But introduced noise logically-impossible hit
    -> Debugging.

Toward Slow Control; Present GDL/CDCTRG Control

- Slow Control not ready
- Terminal-based monitor/control

CDCTRG Monitor





GDL Monitor

Input bits

```
trgadmin@vmetrg18:~ — ssh -XY bdaq.local.kek.jp — 161×50
trgadmin@vmetrg18:~ — ssh -XY bdaq.local.kek.jp
i: input rates
I: input Counts
f: ftd   rates
F: ftd   Counts
p: psn   rates
P: psn   Counts
g; general info
c; clear counters

Thu Jul 20 08:30:36 2017 : UT3p xc6vhx380t (RJ DC cpl) : addr=0x8
Firmware     : GDL  1625 : status=0
Clock source : 125MHz external, 250MHz external
Clock counter: 0x00000000-00000000, running about 0 day 0 hrs 0 min 0 sec
FTD     5
GDL     2017_0720_0353_39
ITD     /home/trgadmin/Setup/GDL/data/itd_0009.dat
PSNM    /home/trgadmin/Setup/GDL/data/psn_0016.dat
DAS     /home/trgadmin/Setup/GDL/data/das_0000.dat
RANDOM  /home/trgadmin/Setup/GDL/data/rnd_0000.dat
GENERAL /home/trgadmin/Setup/GDL/data/adm_0000.dat

 0 n_t3_full0          0,     0.0,     0.0  | 24 bha_type2          0,    538.1,     0.0  | 48 top_bb             0,     0.0,     0.0
 1 n_t3_full1          0,     0.0,     0.0  | 25 bha_type3          0,    488.5,     0.0  | 49 top_active         0,     0.0,     0.0
 2 n_t3_full2          0,     0.0,     0.0  | 26 bha_type4          0,    146.3,     0.0  | 50 top_timing0        0,     0.0,     0.0
 3 n_t3_short0         0,     0.0,     0.0  | 27 bha_type5          0,      9.2,     0.0  | 51 top_timing1        0,     0.0,     0.0
 4 n_t3_short1         0,     0.0,     0.0  | 28 bha_type6          0,    533.3,     0.0  | 52 top_timing2        9,     0.0,     0.0
 5 n_t3_short2         0,     0.0,     0.0  | 29 bha_type7          0,    535.9,     0.0  | 53 top_timing3        0,     0.0,     0.0
 6 n_t2_full0          0,     0.0,     0.0  | 30 bha_type8          0,    538.9,     0.0  | 54 n_klm0             0,  62198.8,     0.0
 7 n_t2_full1          0,     0.0,     0.0  | 31 bha_type9          0,    529.4,     0.0  | 55 n_klm1             0,     0.0,     0.0
 8 n_t2_full2          0,     0.0,     0.0  | 32 bha_type10         0,    428.3,     0.0  | 56 n_klm2             0,     0.0,     0.0
 9 n_t2_short0         0,     0.0,     0.0  | 33 n_clus0            0,      0.0,     0.0  | 57 revo               0,  62198.8,     0.0
10 n_t2_short1         0,     0.0,     0.0  | 34 n_clus1            0,      0.0,     0.0  | 58 her_kick           0,     0.0,     0.0
11 n_t2_short2         0,     0.0,     0.0  | 35 n_clus2            0,      0.0,     0.0  | 59 ler_kick           0,     0.0,     0.0
12 cdc_bb              0,     0.0,     0.0  | 36 n_clus3            0,      0.0,     0.0  | 60 bha_delay          0,  62198.8,     0.0
13 cdc_open45          0,     0.0,     0.0  | 37 bg_ecl_veto        0,      0.0,     0.0  | 61 pseude_rand        0,     0.0,     0.0
14 cdc_active          0,     0.0,     0.0  | 38 ecl_timing_fwd     0,      0.0,     0.0  | 62 veto               0,     0.0,     0.0
15 cdc_timing0         0,     0.0,     0.0  | 39 ecl_timing_bwd     0,      0.0,     0.0  | 63 nimin0            11,     0.0,     0.0
16 cdc_timing1         0,     0.0,     0.0  | 40 ecl_timing_brl     0,      0.0,     0.0  | 64 nimin1             0,     0.0,     0.0
17 cdc_timing2         0,     0.0,     0.0  | 41 ecl_active         0,   1065.1,     0.0  | 65 nimin2             0,     0.0,     0.0
18 e_high              0,     0.0,     0.0  | 42 ecl_timing0        0,    534.9,     0.0  | 66 nimin3             0,     0.0,     0.0
19 e_low               0,     0.0,     0.0  | 43 ecl_timing1        0,    534.3,     0.0  | 67 nimin4             0,     0.0,     0.0
20 e_lum               0,     0.0,     0.0  | 44 ecl_timing2        0,    528.0,     0.0  | 68 nimin5             0,     0.0,     0.0
21 ecl_bha             0,     0.0,     0.0  | 45 n_top0             0,      0.0,     0.0  |
22 bha_type0           0,   540.0,     0.0  | 46 n_top1             0,      0.0,     0.0  |
23 bha_type1           0,   538.0,     0.0  | 47 n_top2             0,      0.0,     0.0  |
```

General Info

```
trgadmin@vmetrg18:~ — ssh -XY bdaq.lo
trgadmin@vmetrg18:~ — ssh -XY bdaq.lo
F: ftd   Counts
p: psn   rates
P: psn   Counts
g; general info
c; clear counters

Thu Jul 20 08:26:29 2017 : UT3p xc6vhx380t (RJ DC cpl) : addr=0x8
Firmware     : GDL  1625 : status=0
Clock source : 125MHz external, 250MHz external
Clock counter: 0x00000000-00000000, running about 0 day 0 hrs 0 min 0 sec
FTD     5
GDL     2017_0720_0353_39
ITD     /home/trgadmin/Setup/GDL/data/itd_0009.dat
PSNM    /home/trgadmin/Setup/GDL/data/psn_0016.dat
DAS     /home/trgadmin/Setup/GDL/data/das_0000.dat
RANDOM  /home/trgadmin/Setup/GDL/data/rnd_0000.dat
GENERAL /home/trgadmin/Setup/GDL/data/adm_0000.dat

gdl0034b
tmdl_busy_length=250,b2l_buffer_delay=5
timsrc=29:top(off),ecl(on),cdc(off),psn(off),random(off)
nimPipeLength=272
top_rvc_offset=0,ecl_rvc_offset=64,cdc_rvc_offset=0
top_rvc_diff=0,ecl_rvc_diff=108,cdc_rvc_diff=0
rvccorrection(on)
 0 commonL1            0,      0.0
 1 theL1          218783,     96.1
 2 top_timing          0,      0.0
 3 ecl_timing     218783,     96.1
 4 cdc_timing          0,      0.0
 5 psn_timing          0,      0.0
 6 rnd_riming          0,      0.0
 7 duration         2276
```

PSNM bits

```
Thu Jul 20 08:26:17 2017 : UT3p xc6vhx380t (RJ DC cpl) : addr=0x8
Firmware     : GDL  1625 : status=0
Clock source : 125MHz external, 250MHz external
Clock counter: 0x00000000-00000000, running about 0 day 0 hrs 0 min 0 sec
FTD     5
GDL     2017_0720_0353_39
ITD     /home/trgadmin/Setup/GDL/data/itd_0009.dat
PSNM    /home/trgadmin/Setup/GDL/data/psn_0016.dat
DAS     /home/trgadmin/Setup/GDL/data/das_0000.dat
RANDOM  /home/trgadmin/Setup/GDL/data/rnd_0000.dat
GENERAL /home/trgadmin/Setup/GDL/data/adm_0000.dat

 0 zzx                 0,     0.0,     0.0  | 11 random             0,      0.0,     0.0  | 22 oup22              0,     0.0,     0.0
 1 ffs                 0,     0.0,     0.0  | 12 bg                 0,      0.0,     0.0  | 23 oup23              0,     0.0,     0.0
 2 zx                  0,     0.0,     0.0  | 13 ecltiming         10,     96.1,    96.1  | 24 oup24              0,     0.0,     0.0
 3 fs                  0,     0.0,     0.0  | 14 nim0               0,      0.0,     0.0  | 25 oup25              0,     0.0,     0.0
 4 hie                 0,     0.0,     0.0  | 15 nima03             0,      0.0,     0.0  | 26 oup26              0,     0.0,     0.0
 5 c4                  0,     0.0,     0.0  | 16 nimo03             0,      0.0,     0.0  | 27 oup27              0,     0.0,     0.0
 6 bhabha              0,     0.0,     0.0  | 17 nima45             0,      0.0,     0.0  | 28 oup28              0,     0.0,     0.0
 7 bhabha_trk          0,     0.0,     0.0  | 18 nimo45             0,      0.0,     0.0  | 29 oup29              0,     0.0,     0.0
 8 gg                  0,     0.0,     0.0  | 19 eclnim0            0,      0.0,     0.0  | 30 oup30              0,     0.0,     0.0
 9 mu_pair             0,     0.0,     0.0  | 20 eclnima03          0,      0.0,     0.0  | 31 oup31              0,     0.0,     0.0
10 revolution          0,     0.0,     0.0  | 21 eclnimo03          0,      0.0,     0.0  |
```

To be included in SC

For shifter's Operation (Plan)

- A few pages, unified trigger windows
  - Hide sub-triggers as much as possible from shifters
  - "ready/not ready" signals with initialization button
  - Unified initialization button hopefully
- Change of pre-scale values in two ways;
  - Change of specific bit
  - Configure all bits with a file

Summary and Plan

- Timing Shift Observed
  - Timing Monitor Ready
- Short Term Plan
  - Update of b2l and b2tt
  - Belle-like bit map in DQM
  - Introduce Random triggers
  - Slow Control
- Long Term Plan
  - KEKB information, Beam Injection veto
  - DAS (Don't Abort Signal)

Input bits from subtrigger

	nbits	name	
CDC	3	n_t3_full	#of 3D full tracks
	3	n_t3_short	#of 3D short tracks
	3	n_t2_full	#of 2D full tracks
	3	n_t2_shoft	#of 2D short tracks
	1	cdc_bb	back-to-back topology
	1	cdc_open45	45 deg opening angle
	3	cdc_timing	timing signal
ECL	1	e_high	1 GeV or more
	1	e_low	0.5 GeV or more
	1	e_lum	3 GeV or more
	1	ecl_bha	
	11	bha_type	Identified as Bhabha
	4	n_clus	# of cluster
	1	ecl_timing	timing signal
TOP	3	n_hits	# of top hits
	1	top_bb	back-to-back topology
	1	top_active	Top Timing active
	3	top_timing	Top Timing
KLM	3	n_klm	# of klm hits
Random	1	revo	
	2	rand	
	1	periodin	1 MHz
	3	bhabha_delay	
NIM	6		TSF/2D inputs

GDL firmware

- Compile OK, no timing error, but did not work well
  - Connection between GDL and ETM not made
  - Prescale values not set or set to non-zero value
  - Unexpected signals

Trigger B2L Data

		#UT3	Phys	Debug	bit/ev	MB/sec	
GDL		1	1	1	30k	115	
GRL		1	1				
ECLTRG		1	1	1	400	11	
KLMTRG		1			7/muon	0.2/muon	Sent to GRL
TOPTRG		2					No b2l? To GRL?
CDC	TSF	9		1			
CDC	2D	4		1			
CDC	3D	4					
CDC	NN	4					
CDC	ETF	1					No b2l?
Total		28					

Status