DHH Status Report

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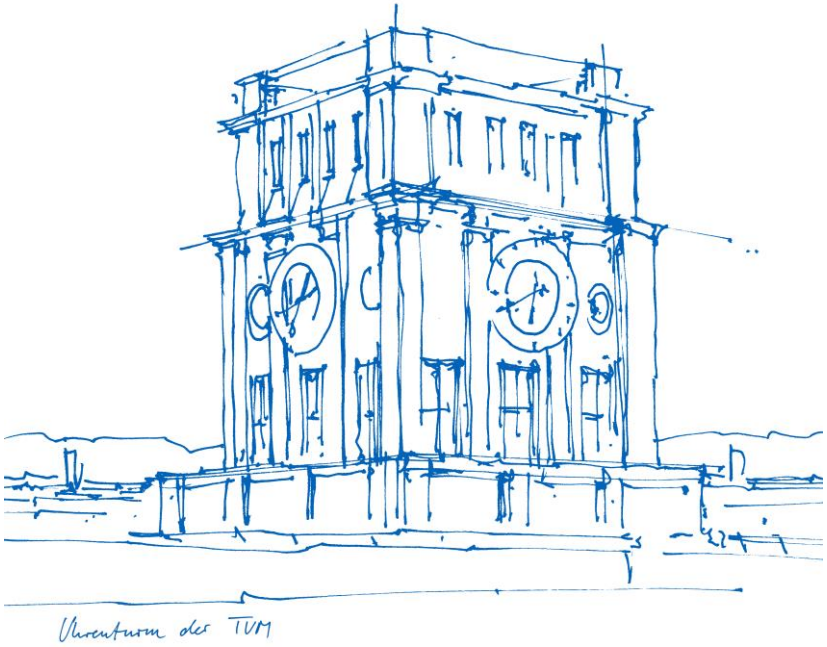
Belle2 DAQ/Trigger Workshop

August 23-25

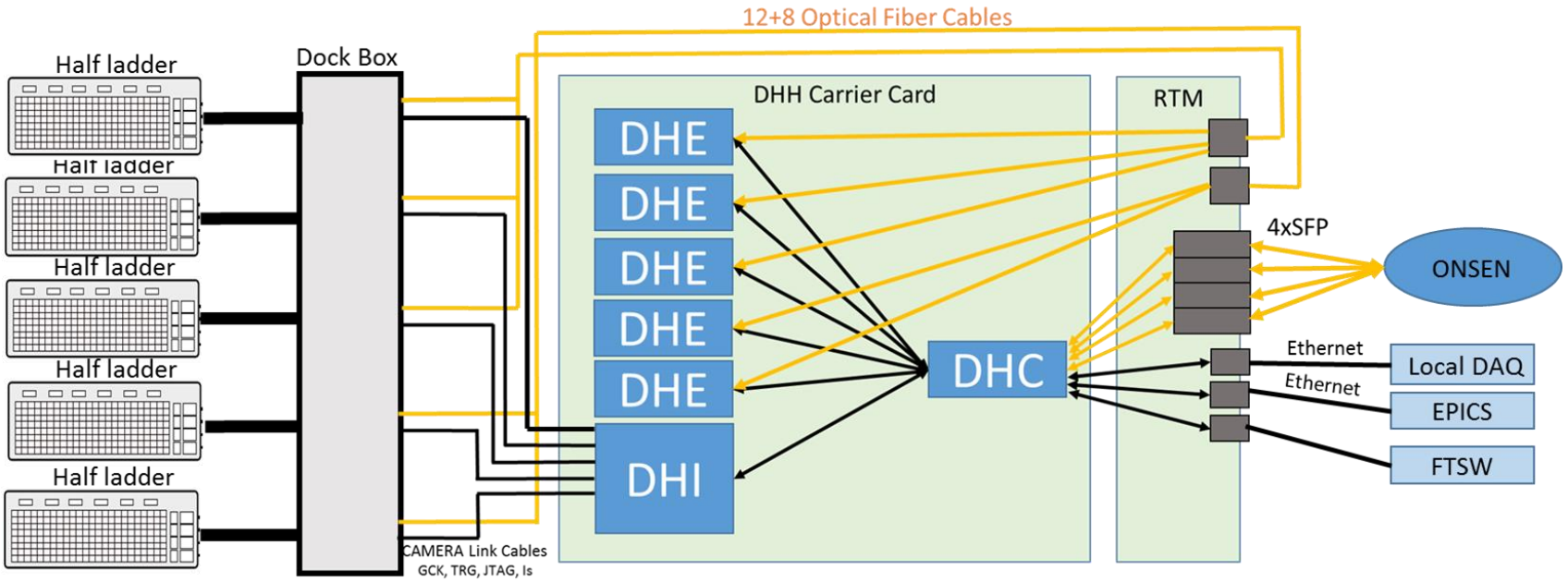
Taipei



Overview

- DHH System Overview
- Current Status
  - High Speed Link Issues
  - Data Handling Hub Hardware
  - Data Handling Hub Firmware
    - UCF
    - DHE
    - DHC

DHH System

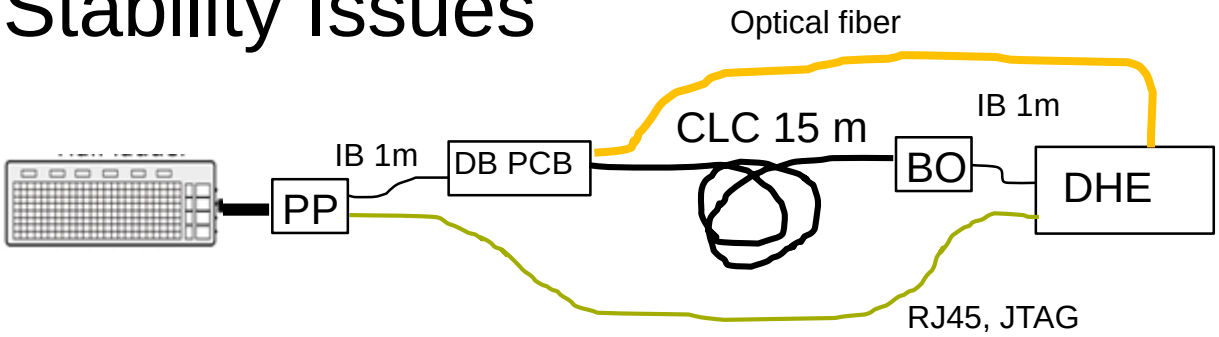


DHHCarrierCard houses 5xDHE, 1xDHI, 1xDHC

External Interfaces are connected via DHRTM module

PXD requires 8 DHHCC

High Speed Link Stability Issues



Instability of data link between detector module and DHE

Many improvements of high speed links:

- Copper links exchanged by optical fibers
- CML driver bug fixed => DHPT1.2b
- Kapton cable design optimized for high speed transmission

Many other parameters contribute to link instability:

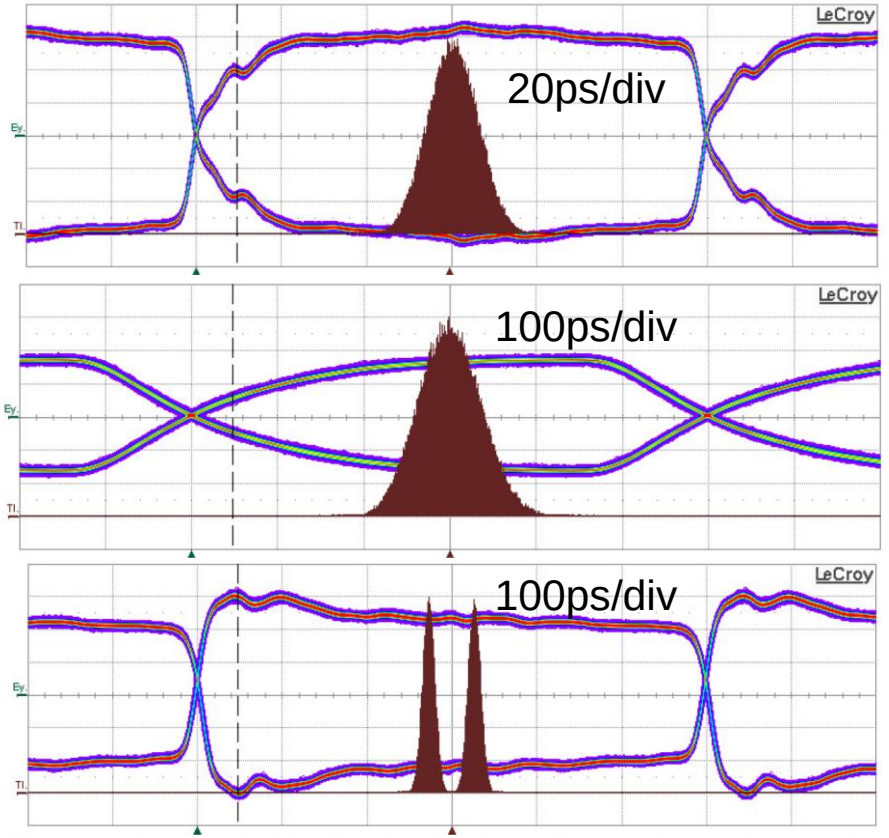
- Imperfection in transmission lines and termination
- Ground and cable shielding to minimize Common Mode Noise
- GCK clock quality
- Phase relation between GCK and TRG line

Improving GCK Quality

GCK clock after 1m of Infiniband cable
Links stable over long period of time

15m of Camera Link Cable (28AWG)
Links unstable

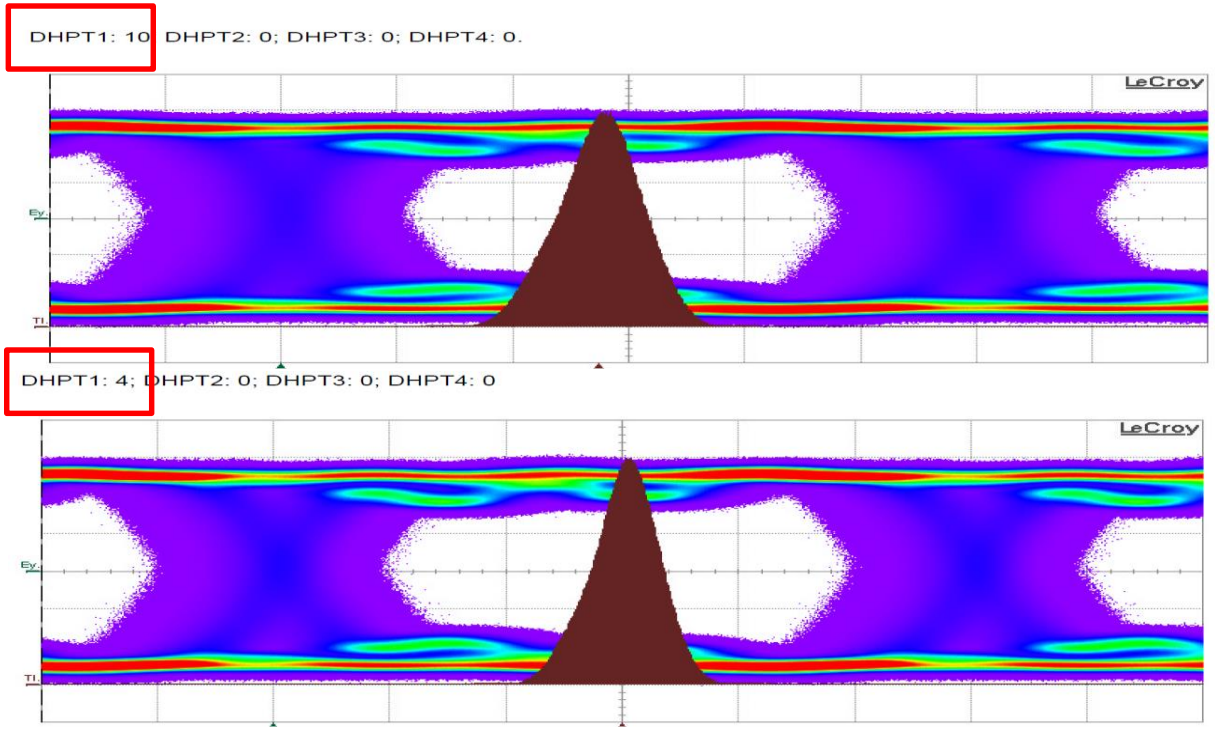
LVDS buffer added to Dock Box PCB
to recover signal shape



One more circuit based on CMOS driver is under tests. This driver is placed on DHE side.

GCK vs TRG Phase Optimization

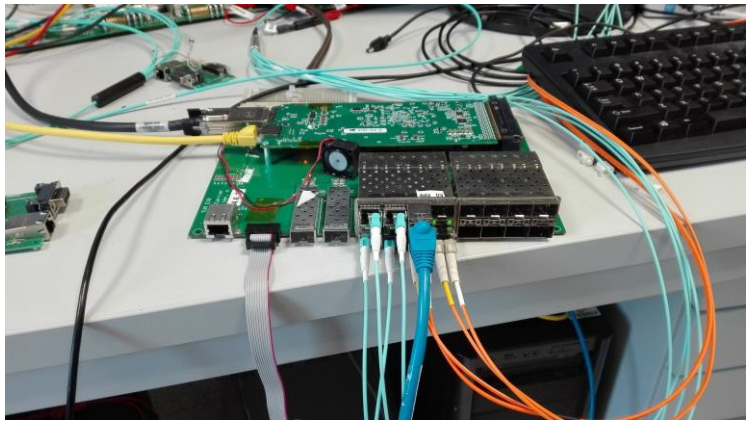
DHPT1.2b allows to change phase relation between GCK and Manchester encoded TRG command in 16 steps.
We found out that the phase relation has an impact on EYE diagram.
After scan of all values we selected those which have narrow and symmetrical distribution.

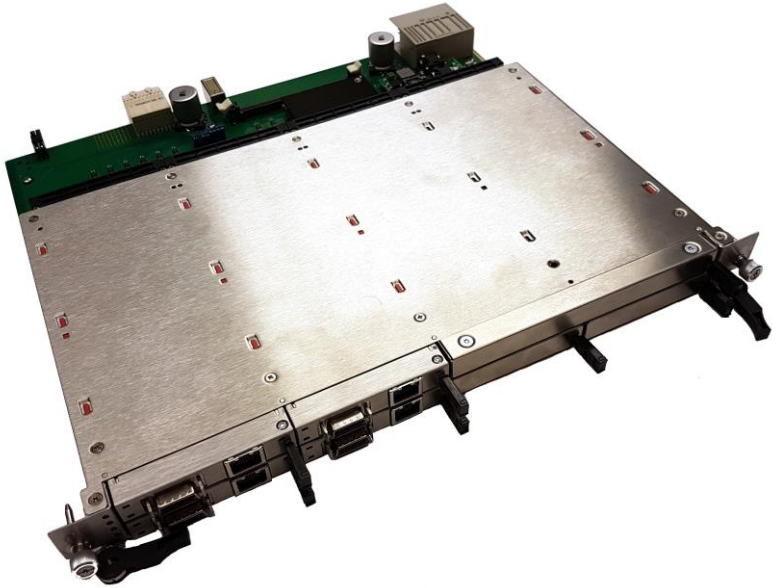


After phase optimization it's possible to operate links without GCK LVDS buffer

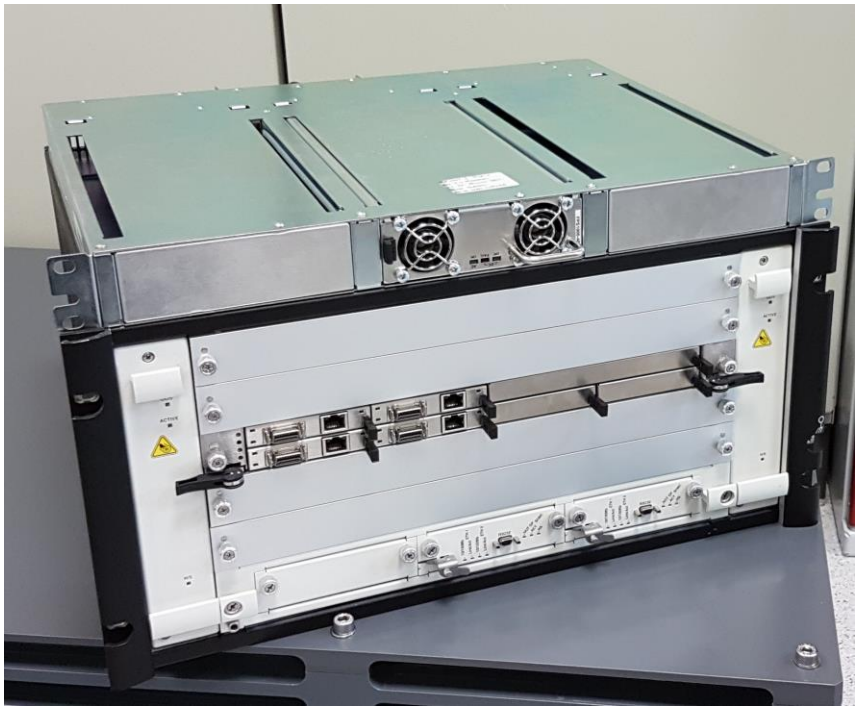
After many optimizations the HS links became stable!

DHH Carrier Card





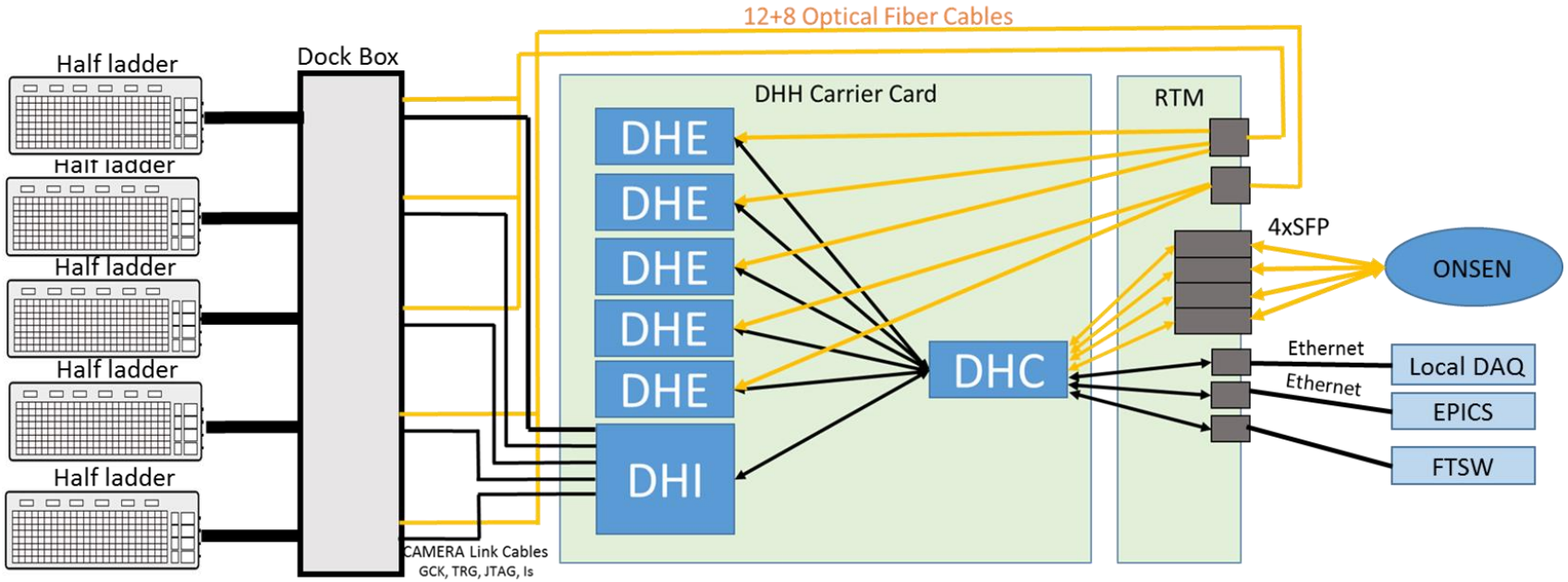
Test of DHHCC and DHHRTM for Phase 2



DHH ATCA card was successfully tested.

Important milestone!

DHHCC Trigger and Data Flow



DHC ⇔ DHE interface is implemented over single Serial link using Unified Communication Framework (UCF) protocol :

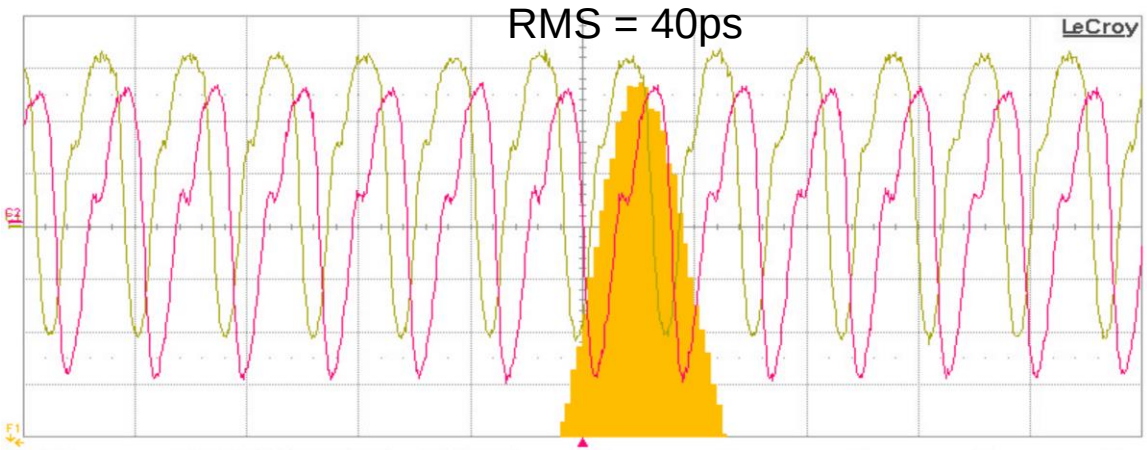
- B2TT clock is a reference clock for serial link
- distribution of B2TT information with fixed latency
- distribution and collection of IPBUS packets for slow control
- Data transmission from DHE to DHC

B2TT Clock and Trigger Distribution Performance

B2TT Clock

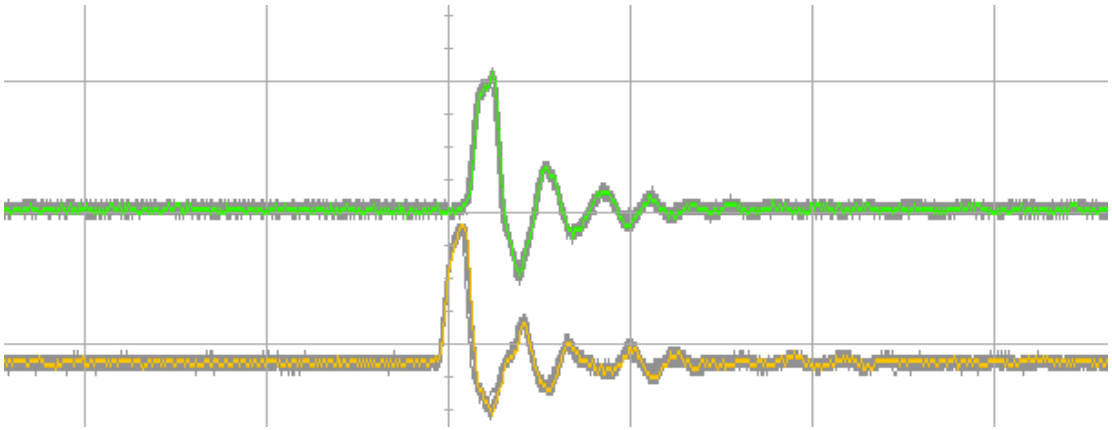
Jitter between recovered B2TT clocks of two DHEs

Phase difference is fixed and does not change after power cycling



Trigger

Time difference between trigger signals of two DHEs has deterministic difference and reproduced after power cycling



DHH Hardware Status

Phase 2

- One DHH ATCA module fully tested and will be tested together with detectors at PERSY.
- Second DHH ATCA will be ready next week.
- DHI module is paused because of problems with High Speed Links, decision to be taken what solution to be followed

Phase 3

- DHH Carrier and RTM cards will be soldered within next two weeks

Firmware Status for Phase 2

Current DHE firmware has limited trigger rate capability of about 5kHz

We plan to provide new firmware, which supports 30kHz trigger rate, in November

Summary

- High speed link stability problem is solved, a decision what solution to take should be done soon
- UCF protocol to transmit B2TT information, Slow Control messages and Detector Data was successfully tested
- Final DHH ATCA module was successfully tested, a second will be tested next week.
- It’s scheduled to ship electronics for phase 2 from DESY to KEK on September 4-th
- DHH hardware for phase 3 will be produced within next two weeks
- DHI modules will be submitted for production as soon as a decision about active circuit to improve GCK signal will be taken
- DHE firmware will be upgraded to handle 30kHz trigger rate befor November

ONSEN

Full Rate ONSEN Test

Is the ONSEN hardware ready
for phase 3?

Hardware and Firmware:
S. Reiter, T. Gessler, D. Getzkow, W. Kuehn, S. Lange, K. Lautenbach (Univ. Giessen)
Z.-A. Liu, J. Zhao (IHEP Beijing)

Slow Control, Run Control, Monitoring:
M. Hoek, C. Sfienti, B. Spruck (Univ. Mainz)

Full Rate ONSEN Test

- Development of hardware finished
- Hardware is in final state
- All boards (carrier and xFP) are manufactured

- Previous tests with small part of hardware
- Previous tests with low data rates
- Previous tests with development firmware

Idea

- Is ONSEN hardware and firmware ready to handle proposed data rate?

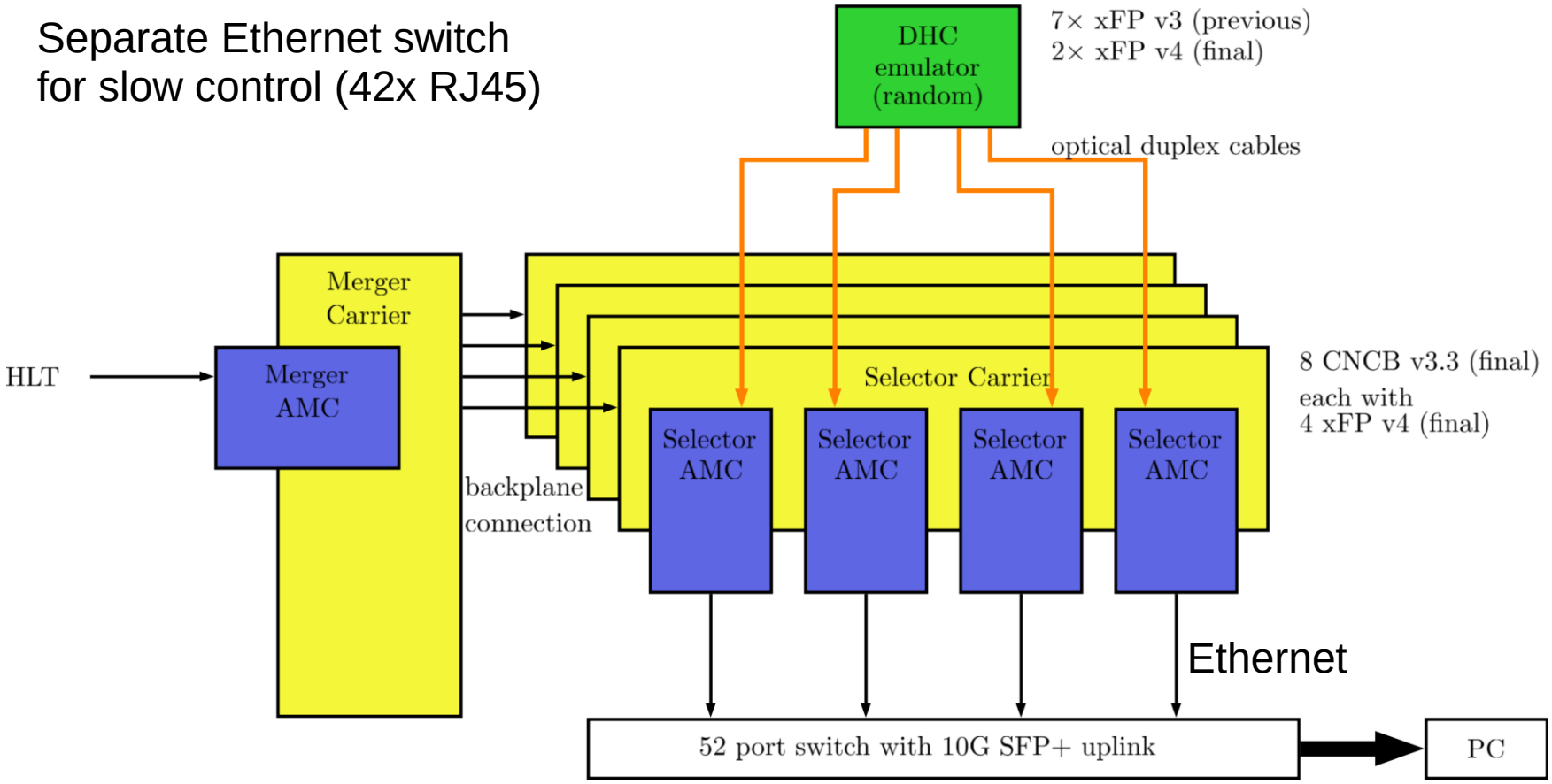
- ~ 550 MB/s input per DHC link
  - ¼ of final trigger rate (7.5 kHz)

total: 17.6 GB/s

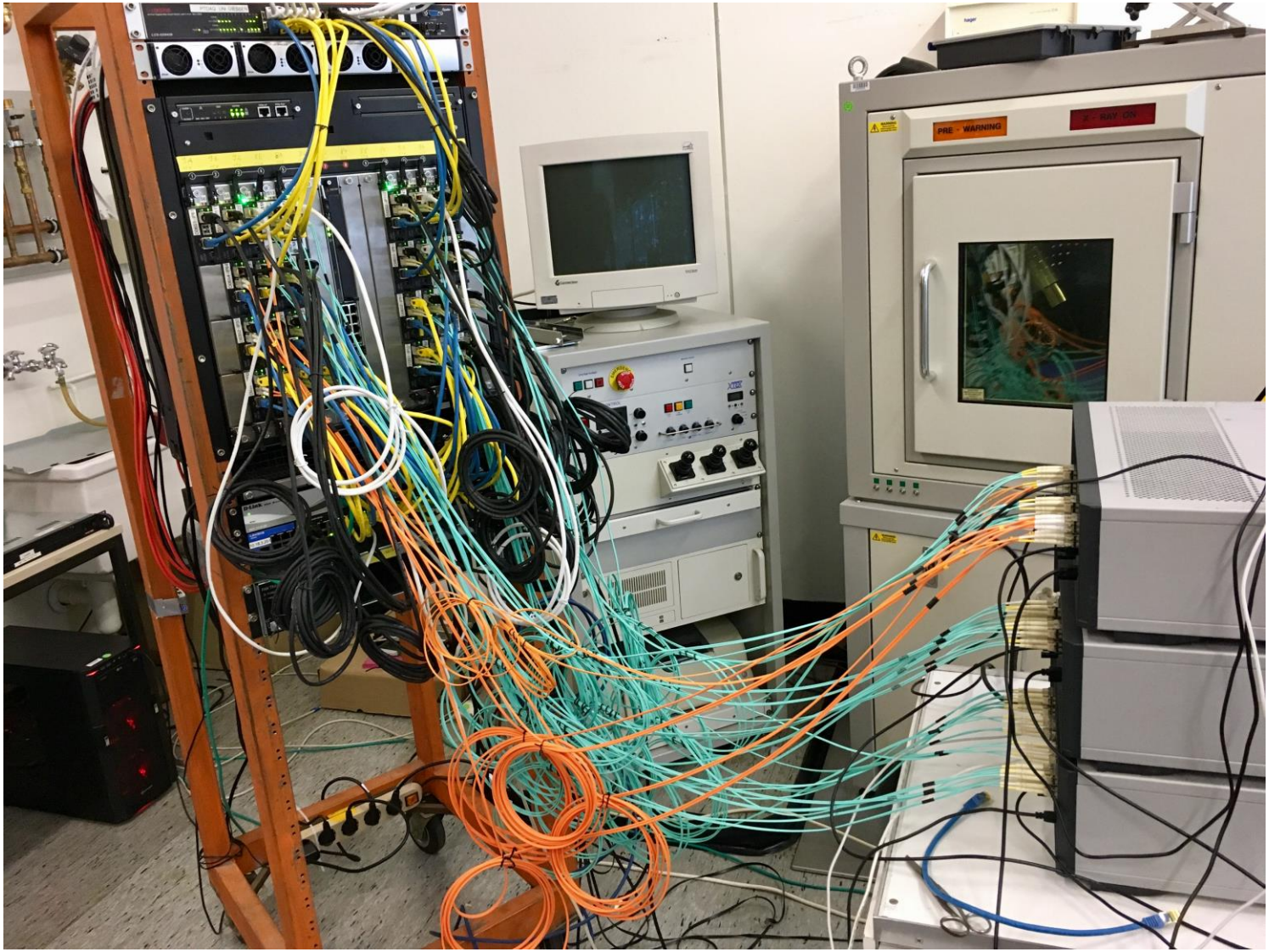
- 7.5 kHz trigger rate of HLT
  - Rejection factor of 2/3
  - No ROI distribution atm.

Schematic Setup

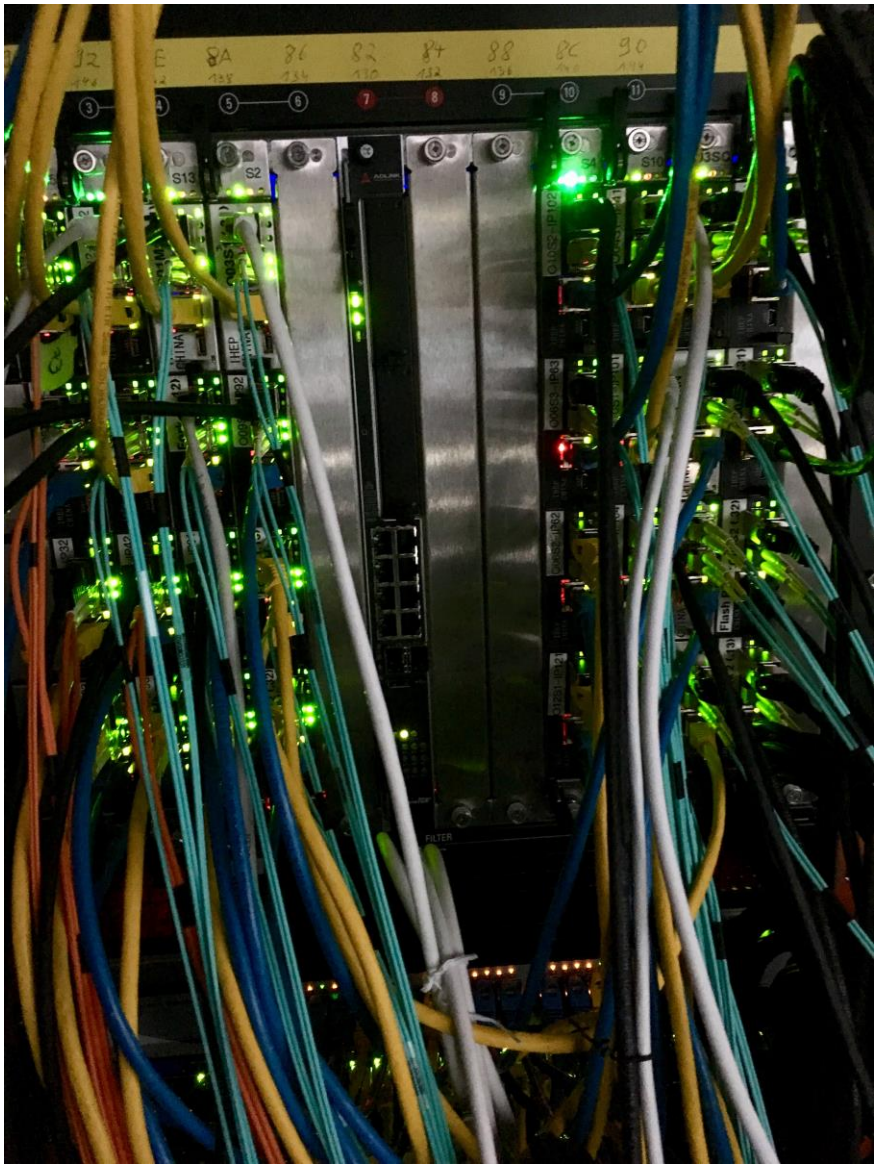
Separate Ethernet switch
for slow control (42x RJ45)



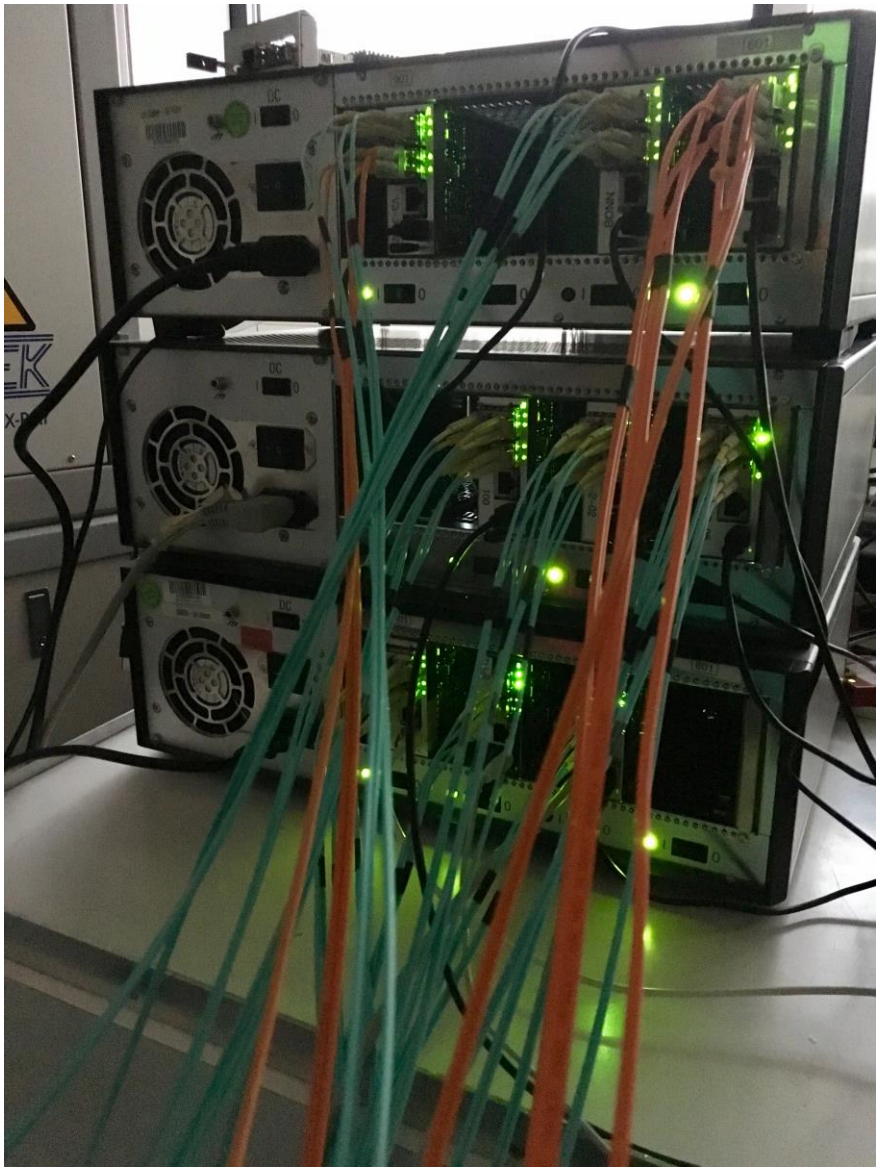
Setup



ONSEN frontal



emulators frontal



Used Data

- ROI generated by software on local PC

with different patterns

  - Send all 0/1
  - Accept 1/3/10
- DHC data with 5 DHE each with 4 DHP
  - 3% occupancy at 6.25 Gbps line rate
  - Random row-column-adc combinations
- Synchronized: HLT(1s delay) & DHC emulator

Test results

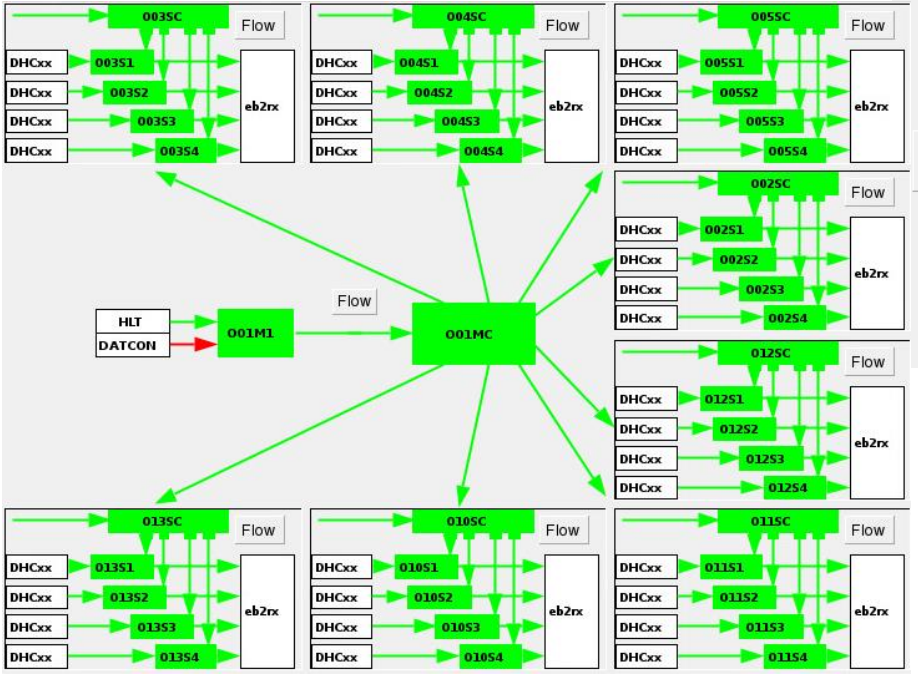
- 3 weeks testing and finalizing software
- No connection interrupts (backplane and ext.)
- No buffer overflows (level ~73%)
- No framing errors / data format errors
- Multiple start/stop without cold start
- Stable temperature in ATCA shelf (FPGA:~60C)

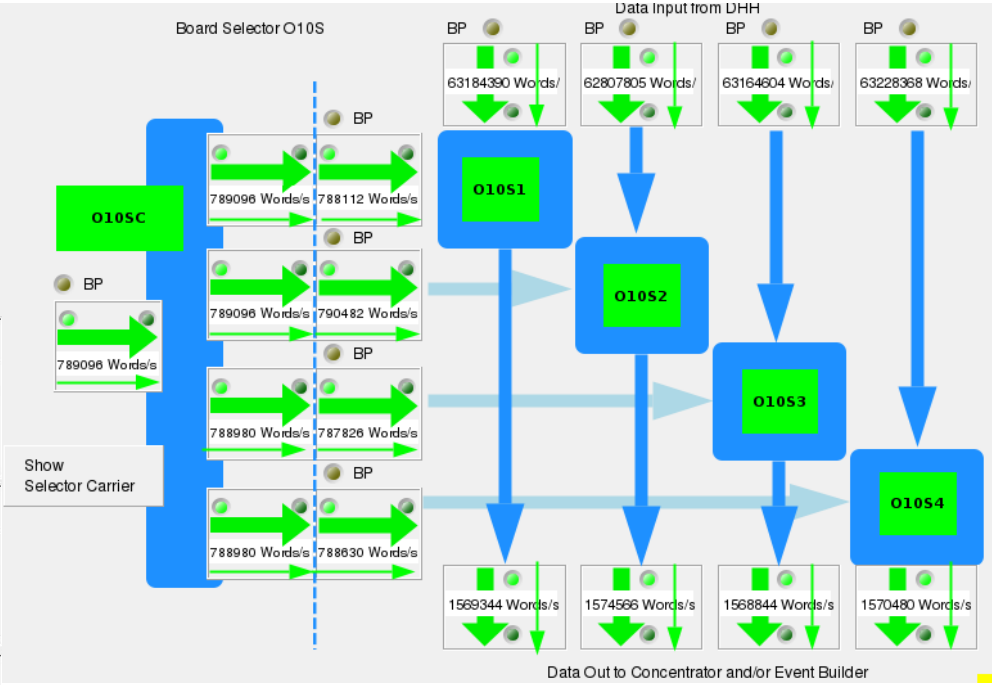
Test results

- Several small runs, storing binary output data on SSD for cross check
- Two long runs over weekend

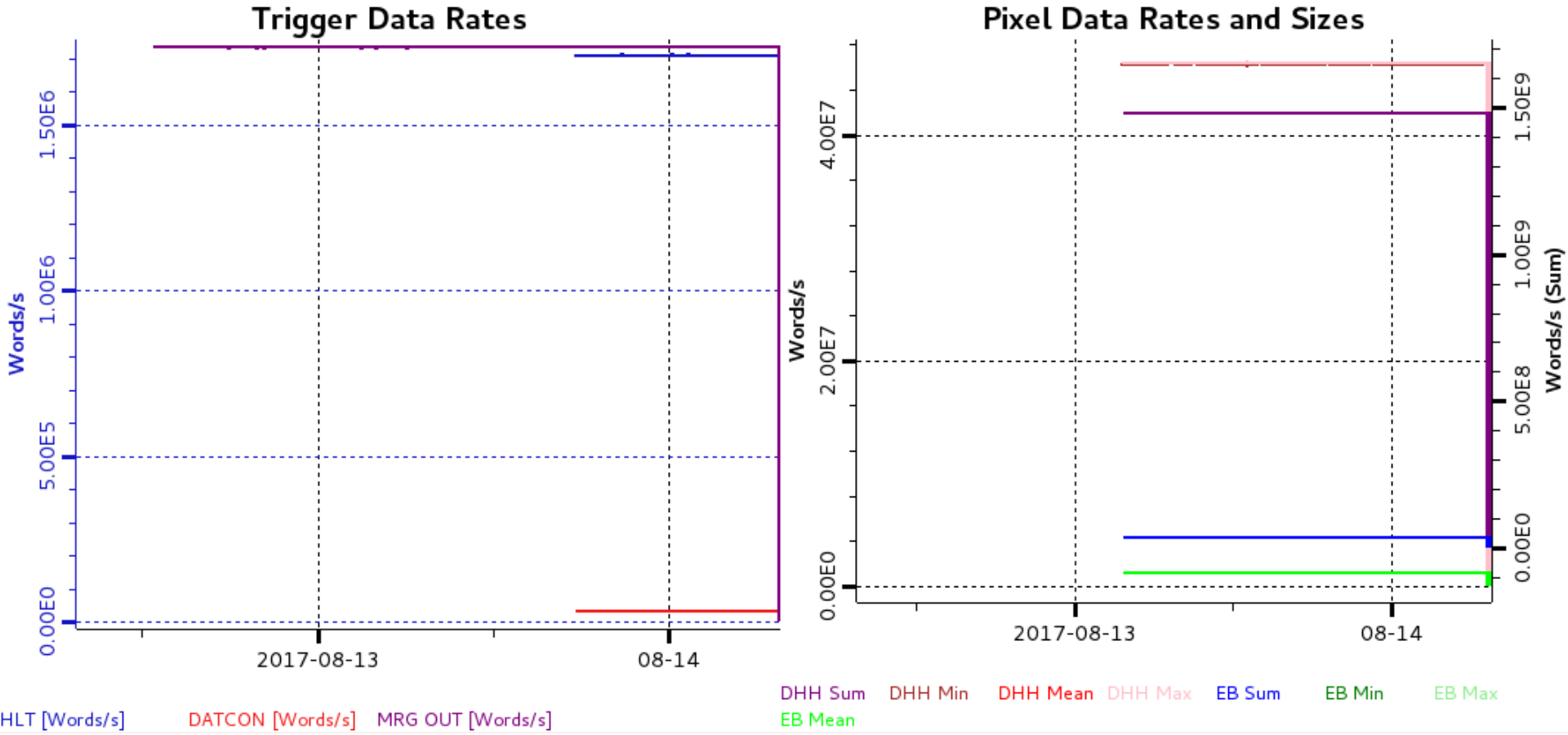
- Maximum trigger rate at 8kHz (limited by DHC aurora line rate): ~595 MB/s
- Send all with reduced data rate of 600 Hz and no rejection factor

Slow Control in CSS





Slow Control in CSS

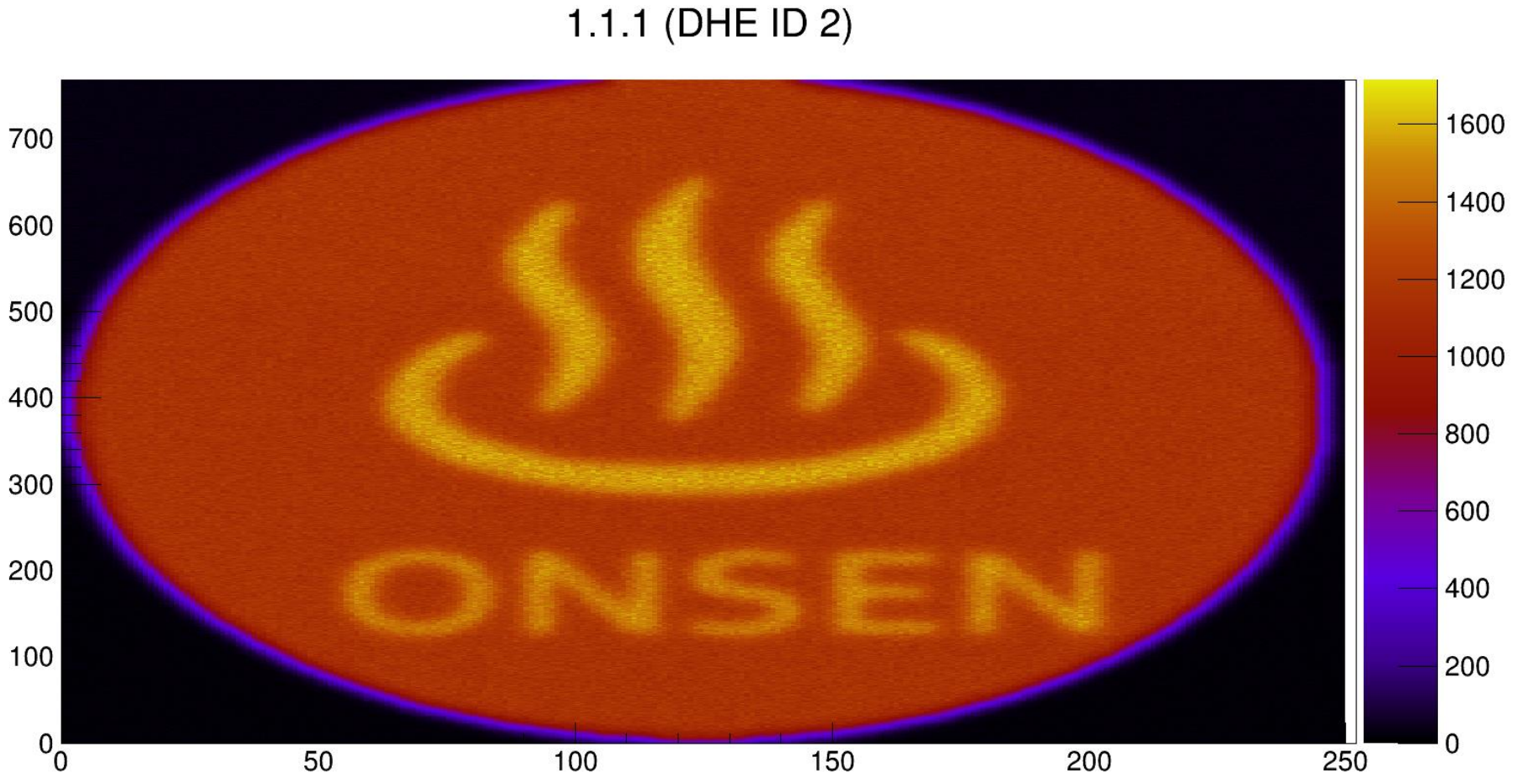


Plan

- August 28 – September 1
  2 carrier with AMC return to DESY (Klemens)
  first time full chain readout of a final PXD module (final ASICs)

- September 18 – 22
  ONSEN phase II integration at KEK (w/o detectors)
  (Deenis and Simon, KEK DAQ group, and members from DHH and PXD RC groups

Thanks for you attention



10 million events

What Limits PXD Trigger Rate

PXD read out system designed to handle 20GB/s, the data rate is a limiting factor for maximum trigger rate

20 GB/s corresponds to 30kHz trigger rate and 3% detector occupancy

Background simulation predicts maximum PXD occupancy of 1%

If detector occupancy is stays at 1% then PXD read out system may process 60 kHz triggers