Belle2link Update

Mikihiko Nakao (KEK)

mikihiko.nakao@kek.jp

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News

- **TOP b2link lost problem is finally understood and solved**
  - Main reason is that the **elastic buffer** of **clock correction** of GTX receiver of Xilinx Zynq FPGA does not work as expected
  - It works for Virtex 5, 6, Spartan 6, not sure for other 7-Series
  - Clock correction is needed because the source (FEE thru TTD from SuperKEKB RF) and destination HSLB (on-board oscillator)
- **How clock correction works**
  - If source clock is slower, destination side inserts extra predifined idle word which can be safely ignored
  - If source clock is slower, destination side removes one word of predefined idle pattern from stream
  - Clock correction status can be monitored by a flag ranging: underflow, below threshold, normal, above threshold, overflow
  - Flag should not show over/underflow if idle patterns are there

Clock correction in Belle2lnk

- **How implemented in Belle2link**
  - 16-bit pattern D00.0 + K28.5 (aka **00bc**) is used as an idle pattern and also for clock correction
  - Other patterns D21.4 + K27.7 and D21.4 + K29.7 (aka **95bf** and **95df**) are used for packet format boundary, but they should not be relevant to the clock correction
- **What was found for SCROD**
  - Kyungho Kim found that extra **95fb** is generated when HSLB clock was slightly slower (reported in 2017.2 B2GM)
  - At the same time, clock correction status was almost always "below threshold" and becomes "underflow" when the extra pattern is inserted
  - Lynn Wood found that **95fb** or **95fd** was lost in SCROD, which means HSLB clock must be faster than RF-derived TTD clock

But then as shown in Kurtis's talk, it was found to be a channel bonding problem?

Channel Bonding (slide added after Kurtis's talk)

Channel bonding is a way to make a trunk of multiple links to send a high data bandwidth data, a function not used in Belle II

- In Virtex-5:

  ```
  TILE_CHAN_BOND_MODE_0 : string := "OFF"; -- "MASTER", "SLAVE", or "OFF"
  ```

  so it is clear that in OFF mode it does not care master or slave
- In Virtex-6 and 7-series (also very similar for Spartan-6):

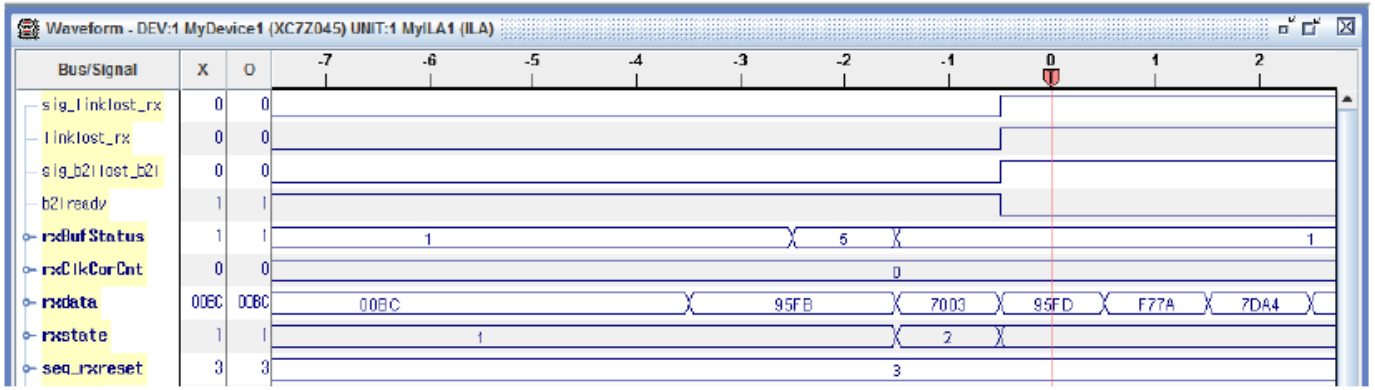
  ```
  RXCHBONDMASTER => '0'
  RXCHBONDSLAVE  => '0'
  ```

  as generated by Xilinx CoreGen, and it works for Virtex-6 and Spartan-6
- In SCROD code, `RXCHBONDMASTER` has to be set to `'1'` (!?). Not sure about other 7-series code, but for Artix-7, CoreGen generates it to be `'0'`.
- ZYNQ GTX code is a part of the SLAC package, not Xilinx code
- Not sure what Xilinx CoreGen generate for ZYNQ, but GTP/GTX coregen for 7-series is very badly designed (IMHO)

Long Time Trigger Test

Long time trigger test

- x"95FB" of rxdata trigger comes twice
- State sequencer goes to 0 and is stopped because sequence for that is not set
- Our solution : Add new sequence that covers this situation
  - After adding, long time trigger test is finished successfully



Trigger shape when x"95FB" comes twice

Workaround and Release

- **Updated belle2link and hslb code**
  - belle2link receiver is updated to ignore second **95fb** and **95fd**
  - Since it is not possible to recover the discarded **95fb** or **95fd** word, HSLB is updated to always generate **two** **95fb** and **95fd** in sequence
  - Therefore, new HSLB is not compatible with old belle2link firmware
  - Second **95fb** and **95fd** should be harmless in other system for Virtex 5, 6 and Spartan 6
- **Release**
  - belle2link 0.19 includes (only) this change w.r.t. belle2link 0.18
  - hslb 0.64 is the new version while previous release was hslb 0.54
  - Previous stable hslb firmware was hslb 0.52
  - Versions 0.55 thru 0.63 are devoted to study COPPER data corruption
  - **New hslb release 0.65 to be released without this workaround** just to keep the latest one to be the production version

Wishlist 1

No time to work on belle2link recently as too much occupied on TTD, but there are many wishlist items

- **Mechanism to study b2llost**
  - Recording the snapshot of data stream is useful to study the cause
  - Needed where no chipscope can be used (e.g. in CDC)
  - Recorded data can be retrieved through belle2link
- **Mechanism to enable non-stop DAQ type restart**
  - after b2lost or data corruption

Wishlist 2

- **Larger event size**
  - HSLB receiver buffer has 32 kword depth, but writing-to-COPPER part is limiting the event size to 8 kword
  - Even worse is that state handling after receiving 8 kword looks incorrect (**probably a bug**)
  - HSLB probably has enough resource for an even larger event buffer
- **Handling of overflowing data stream**
  - Currently the system crashes if FEE sends a data stream larger than the event size
  - Extra data can be just ignored and some flag can be attached to the event trailer
- **and more...**