KLM Front End Electronics

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on behalf of

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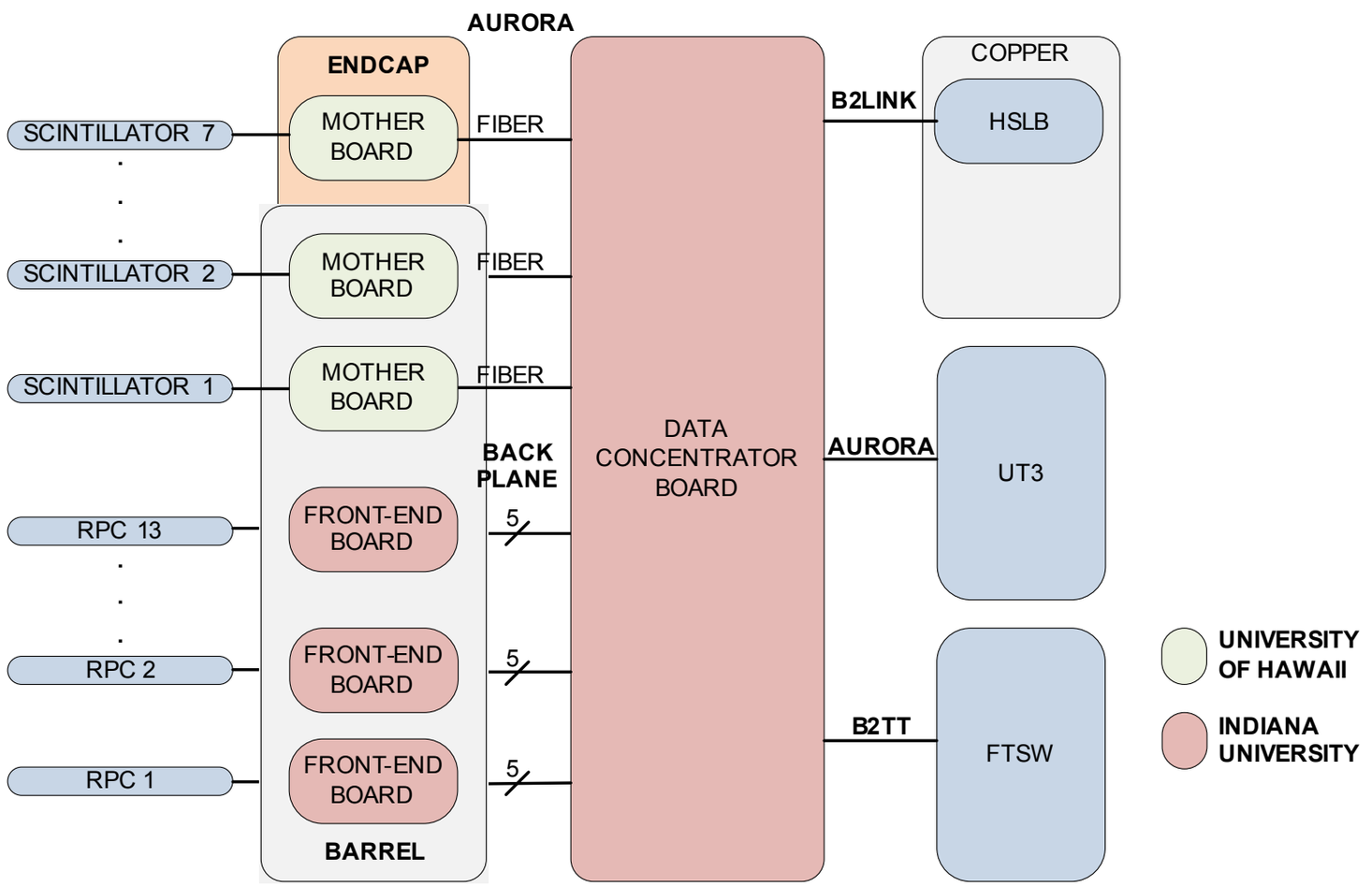
KLM Readout Overview

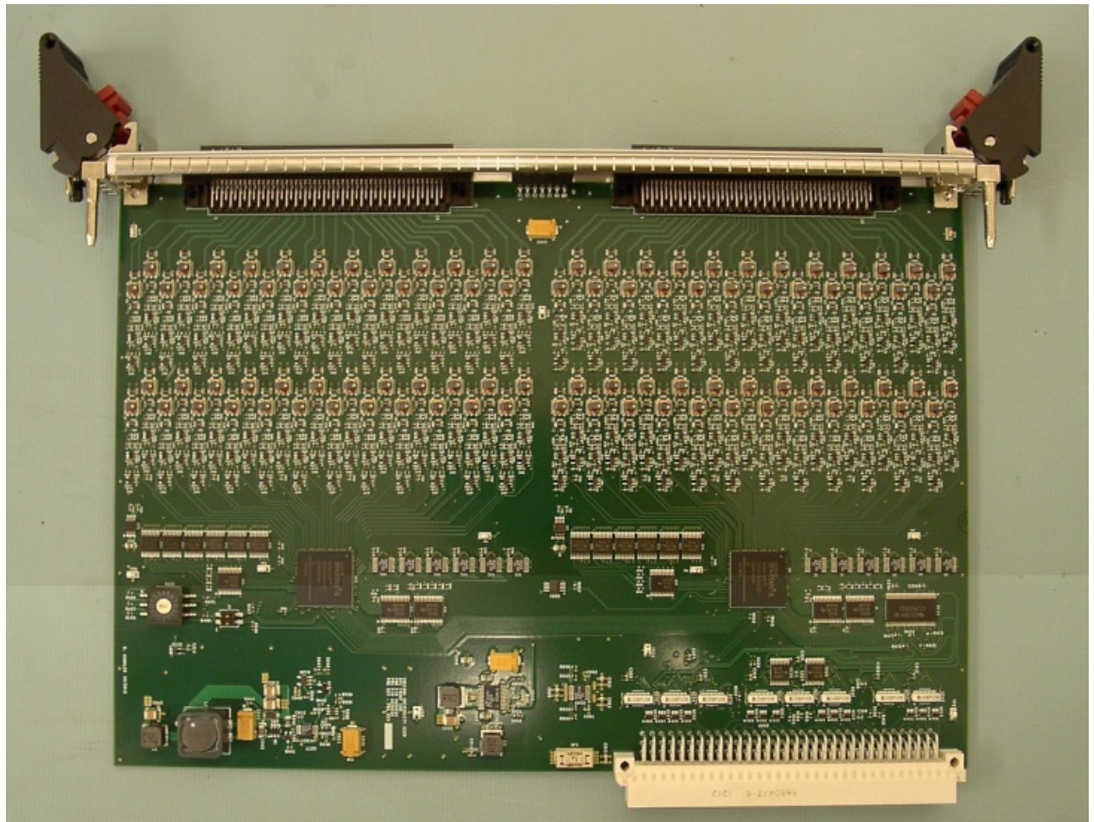
- 13 RPC Front-End boards and 2 Scintillator Motherboards connect to a Data Concentrator in the barrel
- 7 Scintillator Motherboards connect to a Data Concentrator in the end-cap
- The Data Concentrator connects to the detector interface (HSLB, UT3, FTSW)

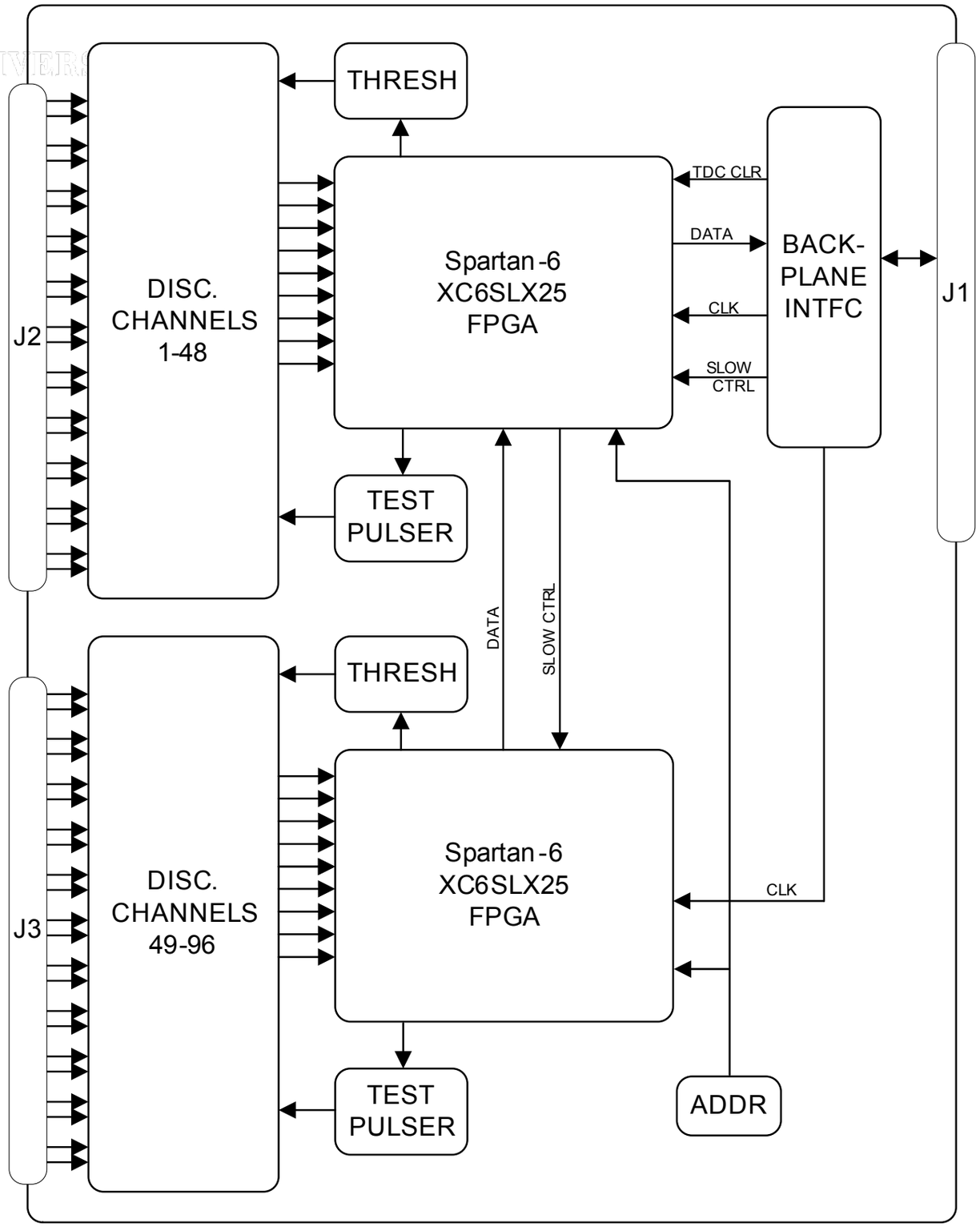
- Indiana University designed the RPC Front-End and Data Concentrator
- University of Hawaii designed the scintillator electronics.



RPC Front-End Board

- 96 line receivers + disc channels.
- Channels 1-48 connect to negative RPC pulses.
- Channels 49-96 connect to positive RPC pulses.
- DAC-controlled discriminator threshold
- Analog test pulser for independent built-in test of each channel.
- Two FPGAs for discriminator control and TDC generation.

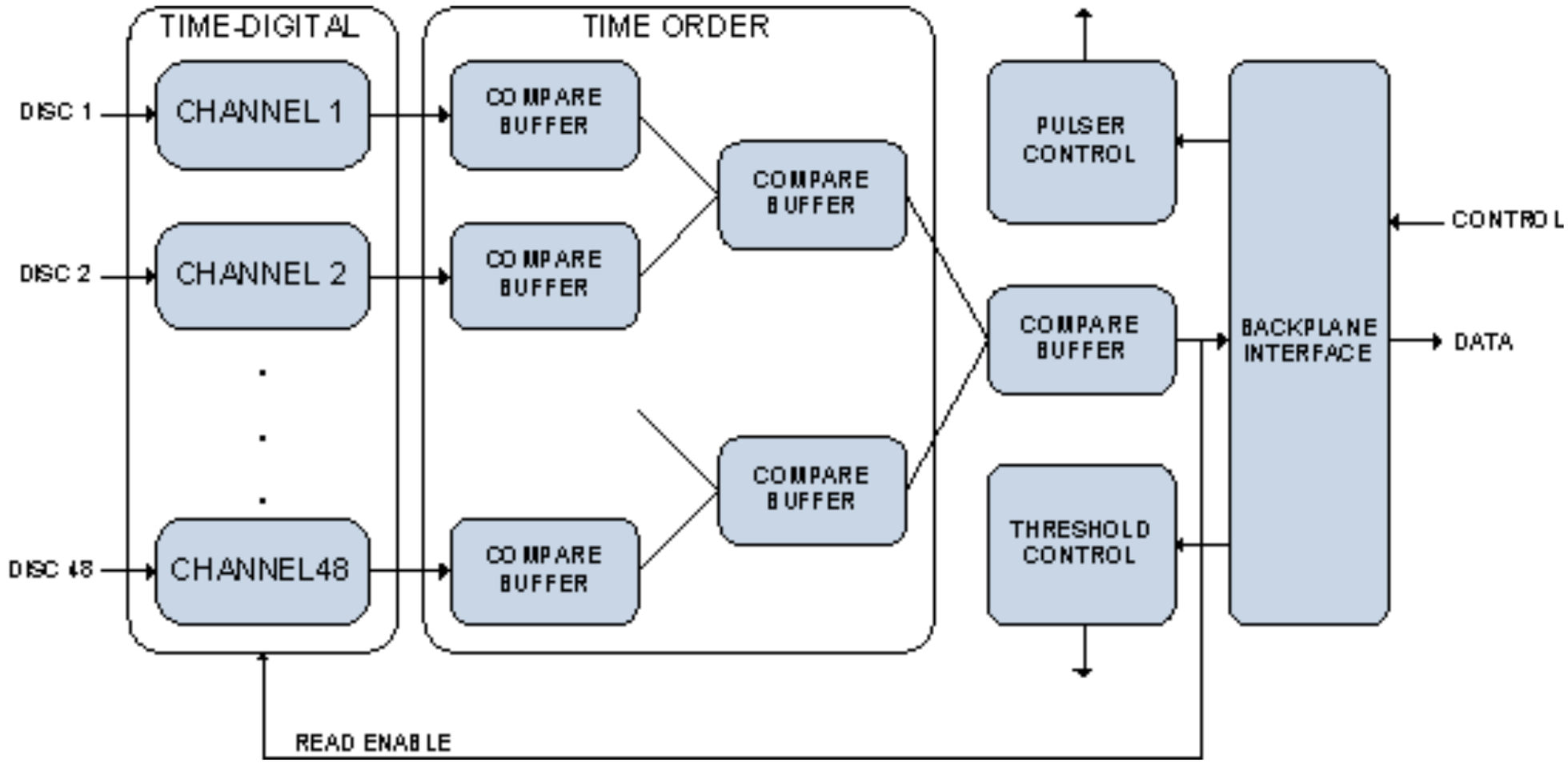




Most of the RPC front-end boards procured by INFN Frascati + Roma 3

RPC Front-End FPGA

- Controls the discriminator threshold and test pulser
- Creates 9-bit fine time (TDC) with a resolution of 3.94 ns (254 MHz)*
- Time orders TDC values to simplify intra-layer coincidence finding on Data Concentrator board
- Transmits TDC values to Data Concentrator board over custom backplane

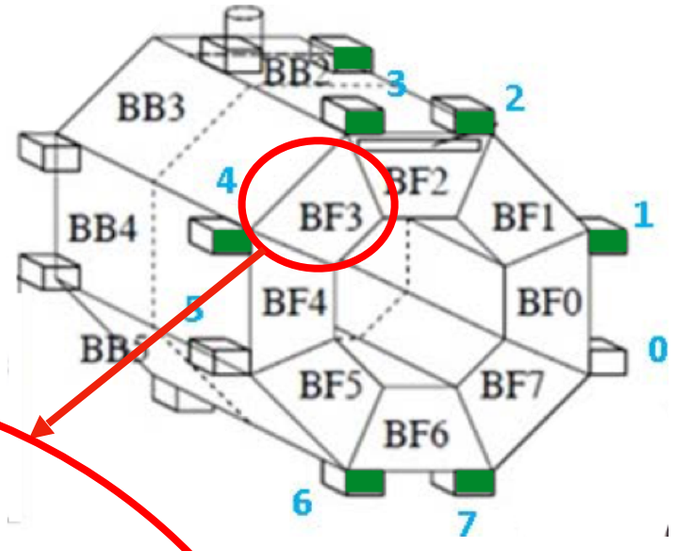


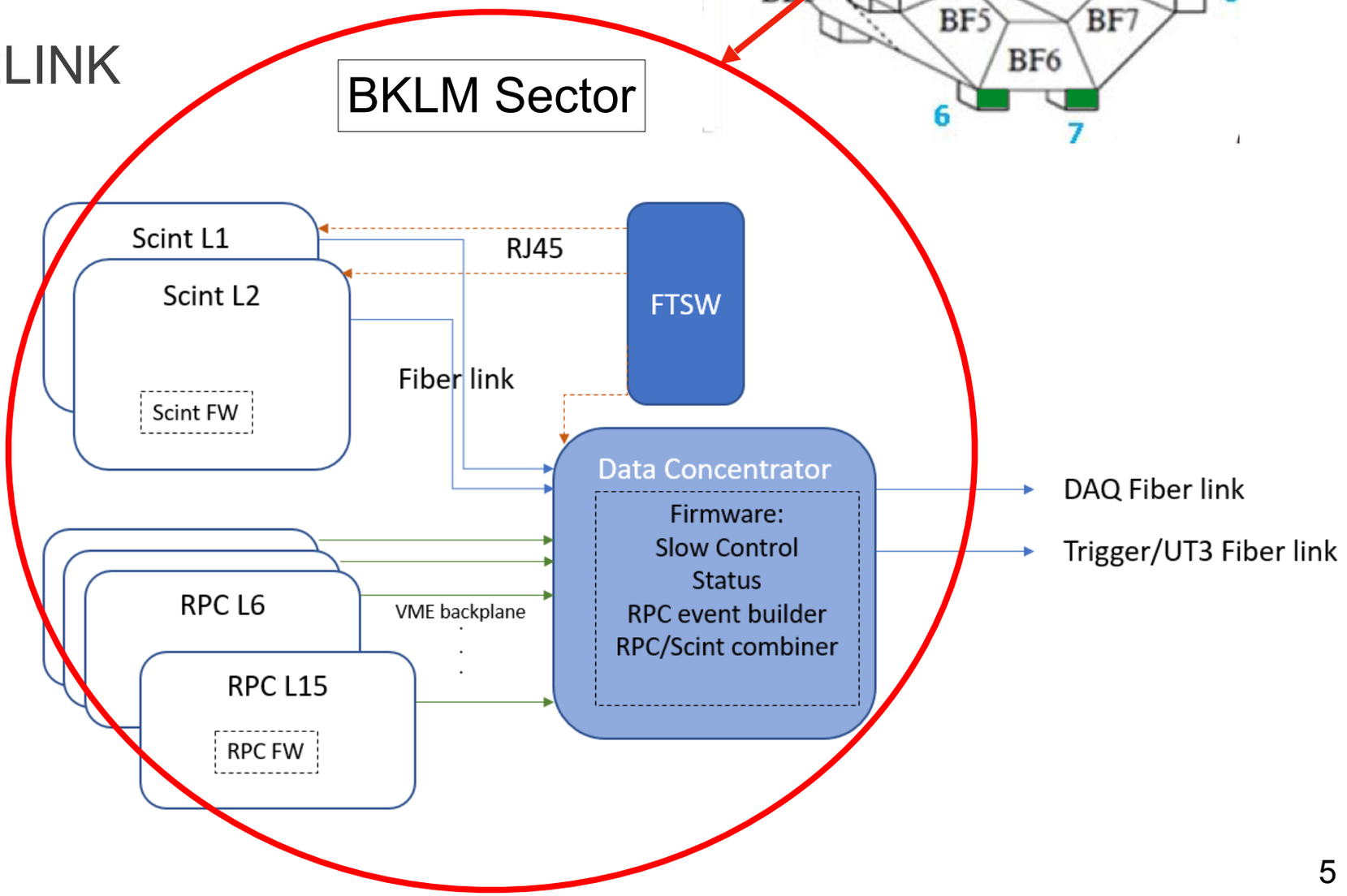
* 2^(9-bits)/(127.216 MHz) = 2.01μs *(1/5 revolution)*

BKLM: Scintillator–MPPC data flow

Hardware unit = 1 BKLM sector (of 16)

- 2 layers of scintillator modules
- 13 layers of RPC modules
- 1 data concentrator to combine data
- Data concentrator runs B2LINK and is in charge of
  - ✓ slow control
  - ✓ status
  - ✓ data aggregation
  - ✓ uplink trigger primitives





EKLM similar except

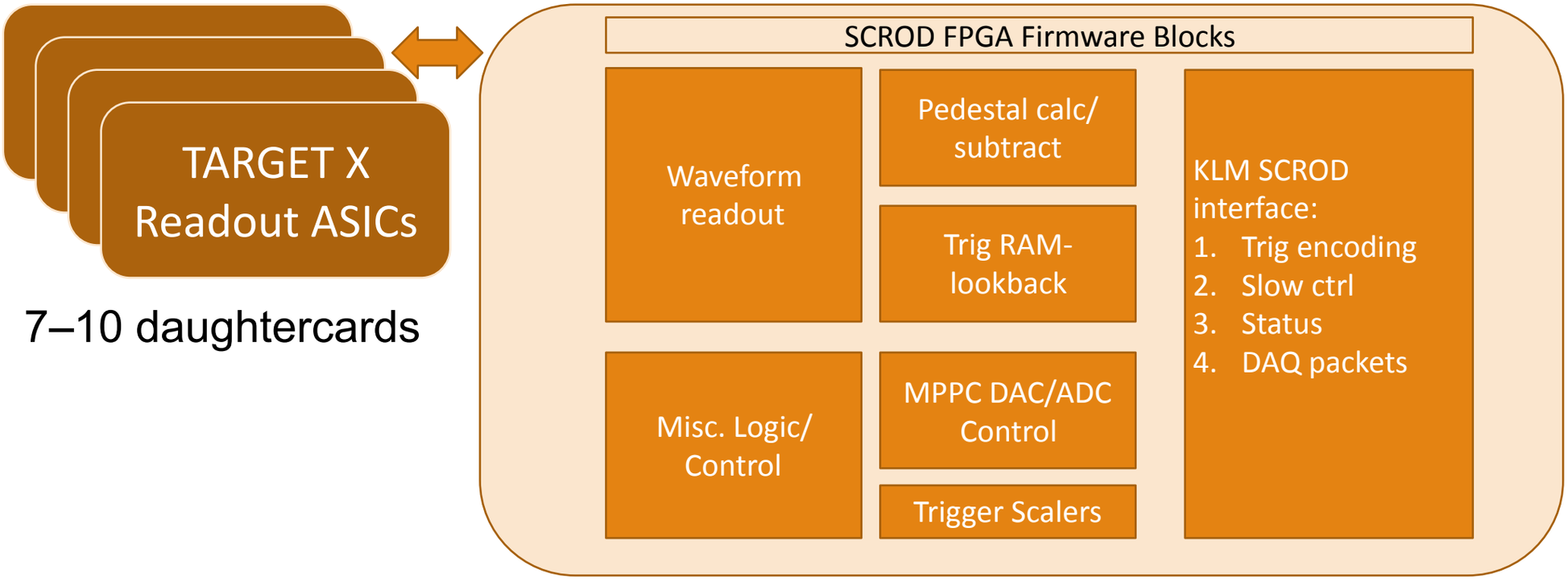
- no RPCs
- 7 scint modules → 1 data concentrator

Scintillator Subsystem and Operation

Each scintillator module consists of 160 readout channels
- ✓ ~70 connected for BKLM, 150 connected for EKLM

Full waveform sampling with region-of-interest readout using TARGETX ASIC

Calibration, feature extraction, and trigger primitive-time encoding on Spartan 6 SCROD FPGAs



1 motherboard

Scint Readout: Sequence of Operation

Power up

Program FEEs (FPGA bit files)

Send Slow Control Config:
1.Calculate pedestals
2.Set MPPC bias
3.Engage for readout

Start data taking:
1. Disable/enable desired sectors
2. Run data taking scripts
3. Send triggers

Initialization

Await FTSW trigger

FEEs look back in trigger primitives (~5us)

Hit?

N

Y

Digitize ROI

Pedestal subtraction

Calculate Q & T

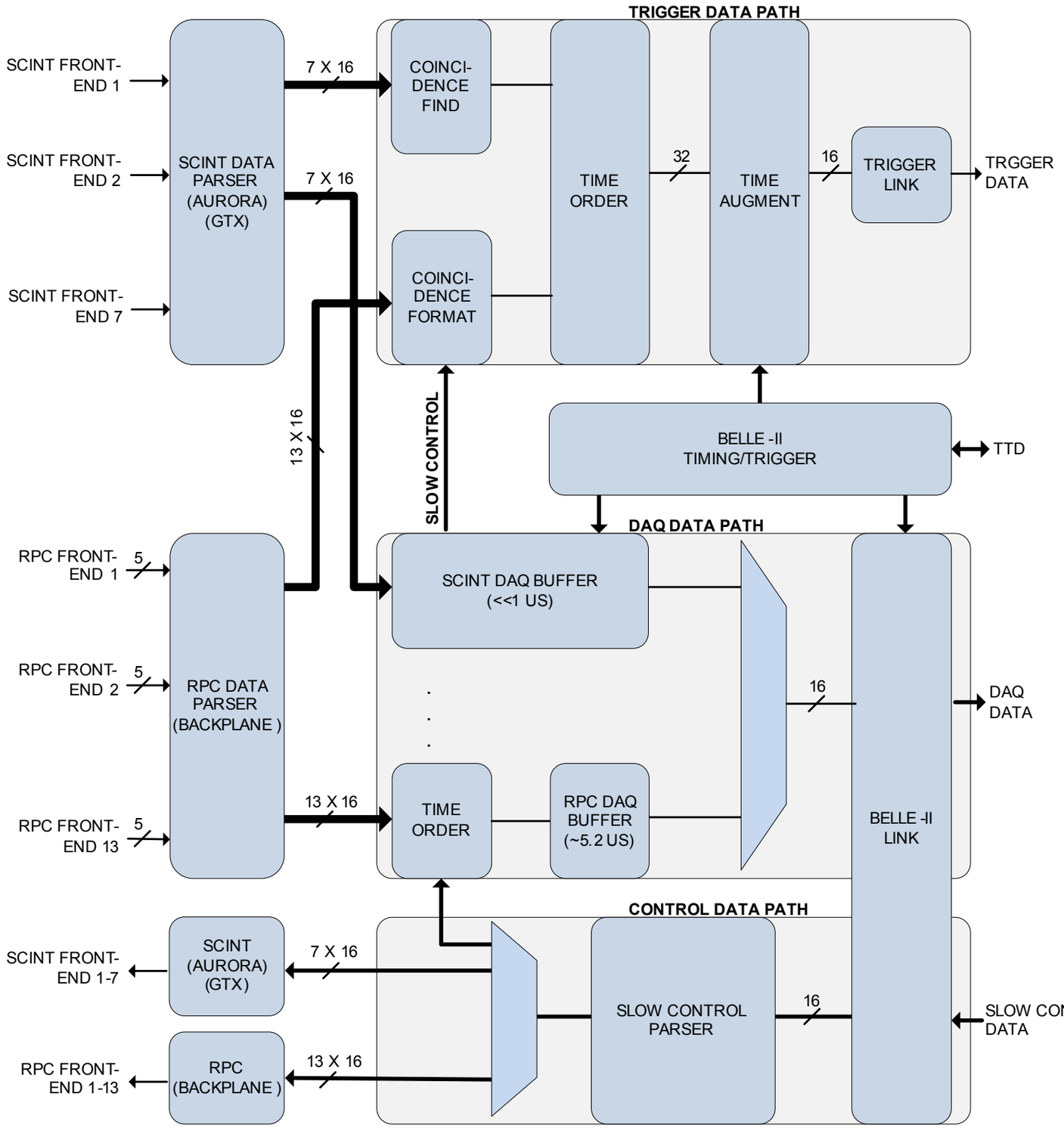
Package and send to Data Concentrator

Data taking

Presently, feature extraction is a simple max-value calculator

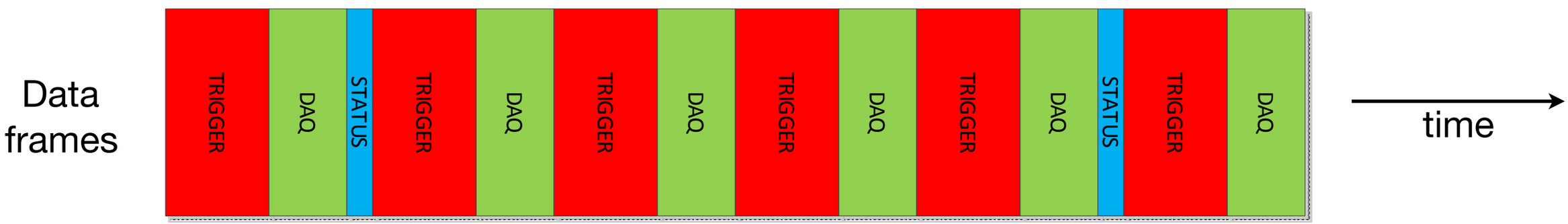
Data Concentrator FPGA

- Interfaces to 13 RPC Front-End boards
- Interfaces to 2 or 7 Scintillator Motherboards
- Interfaces to the DAQ infrastructure (TTD, UT3, ..)
- Performs 3 major functions:
  1. Trigger pre-processing
  2. DAQ data management
  3. Slow-control distribution



Scint. Motherboard – Data Concentrator Interface

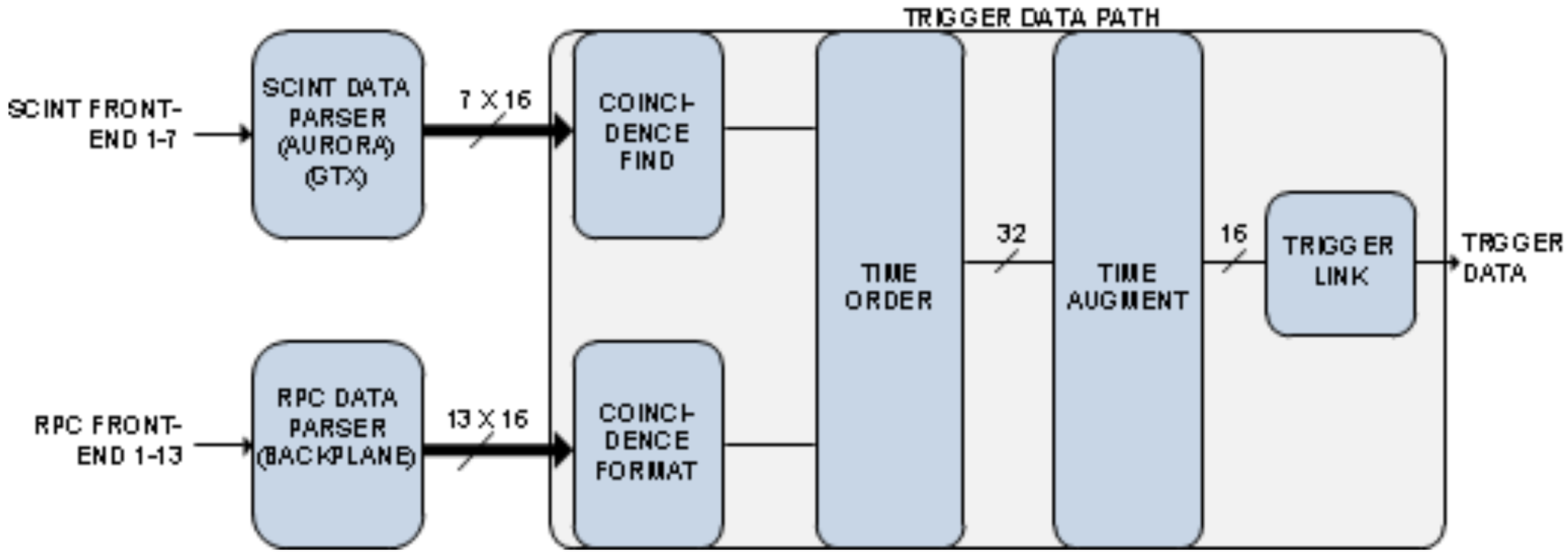
- Seven lanes of scintillator trigger data, DAQ data, and status data flow through a single Data Concentrator.
- Need a protocol for data transmission:
  - Each data type has a time slot (as in communications standards).
  - Trigger data has the largest time slot at >95% to limit delay.
  - DAQ data uses most of the remaining time.
  - A status packet can be sent infrequently – maybe every 2048 trigger packets.
- Implemented with Aurora core framing interface:
  - The SOF signal is asserted at the beginning of a slot.
  - The EOF signal is asserted at the end of a time slot
  - Pauses are used within a time slot if no data is present.
- Deterministic interface that maintains trigger priority, easy to implement, and easy to troubleshoot.



Trigger Data Path

INDIANA UNIVERSITY

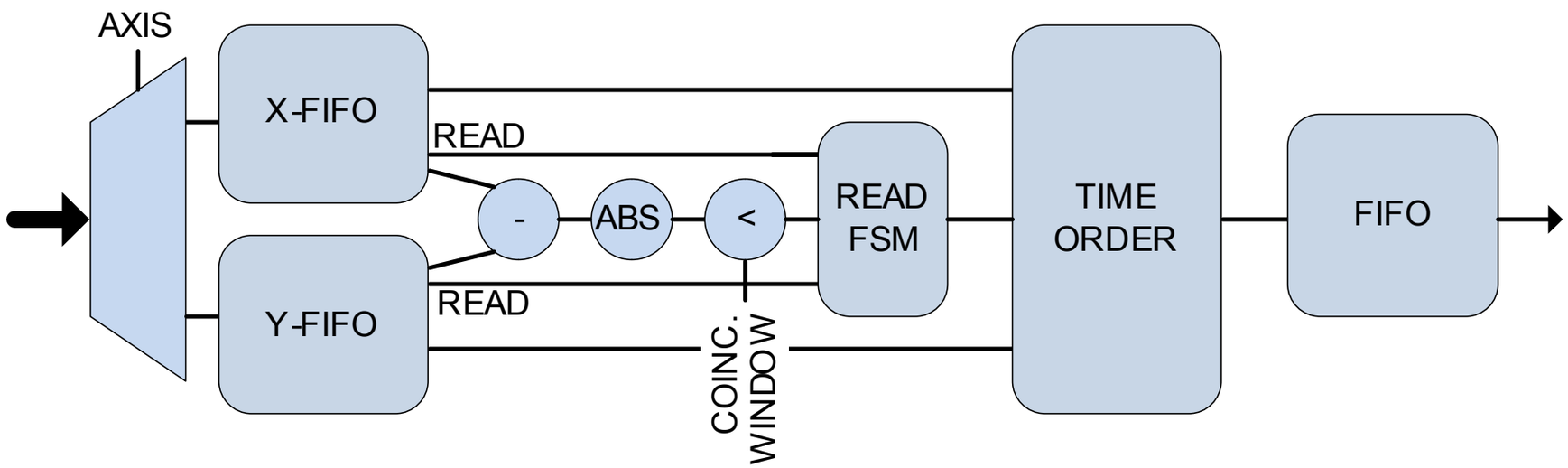
- Parses from Scintillator Aurora interface and RPC backplane to create unified trigger data format.
- Finds coincident hits on orthogonal Scintillator fibers.*
- Formats RPC data to mirror Scintillator coincidence finder output (no coincidence finder on RPC data because always coincident).
- Time orders remaining trigger data – this process also combines data into a single 16-bit trigger data lane UT3 connection.



** currently disabled for debug*

Coincidence Finder

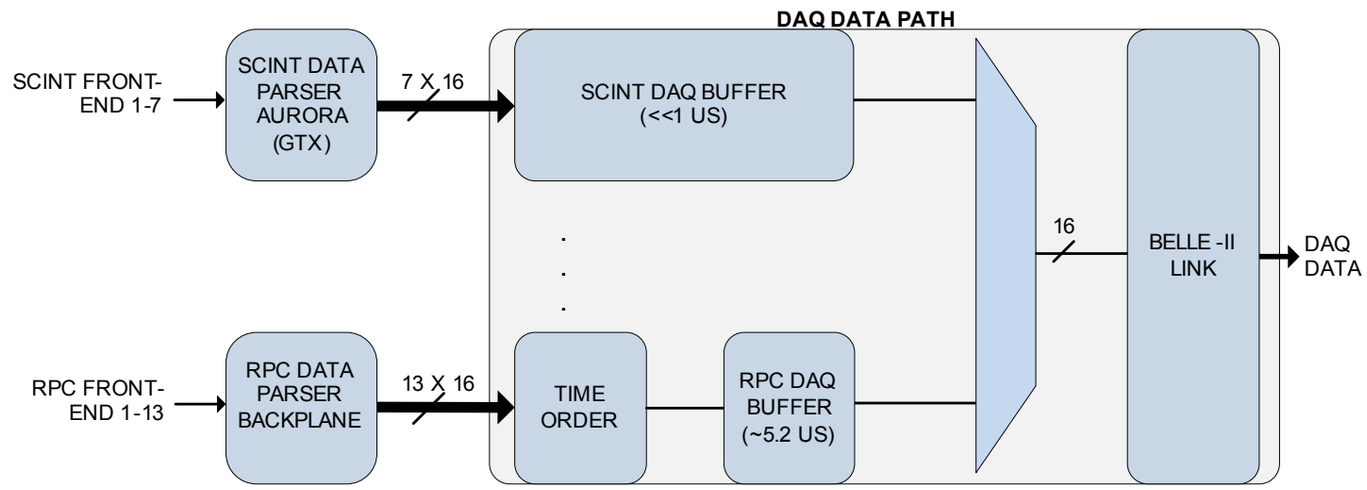
1. Separate channels into respective axis.
2. Test for coincidence.
3. Write both samples to a FIFO if coincident.
4. Read earliest sample if no coincidence.
5. Test for coincidence (repeat)



DAQ Data Path (Event Builder)

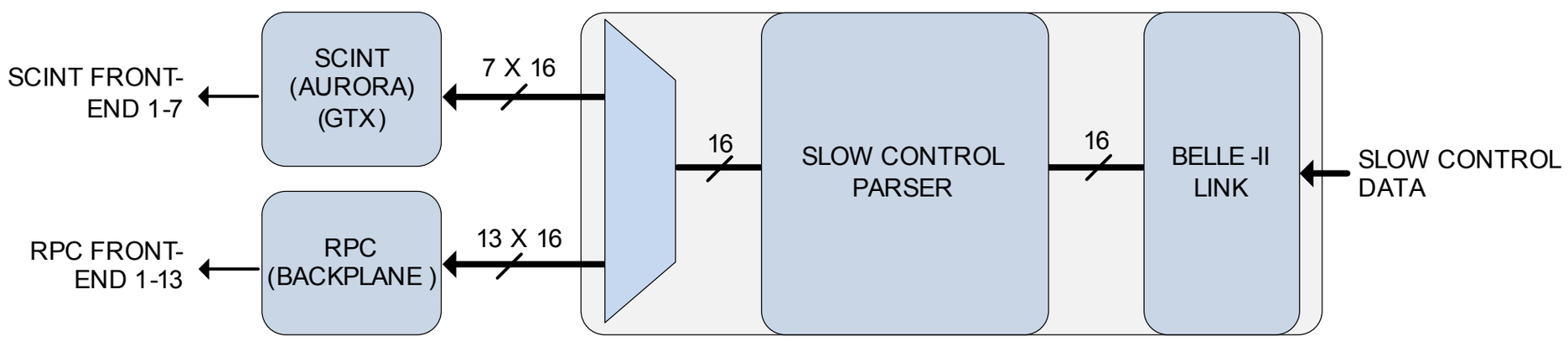
- Augments find-time stamps with truncated CTIME.*
- Parses scintillator and RPC data to creates smaller packets comprised of a single sample (e.g. channel and time word).
- Time orders RPC samples so stale data can easily be removed from buffer.**
- Buffers ~5.2 μs of RPC data while waiting for trigger.
- Buffers scintillator samples for lane combination.
- Combines scintillator events and RPC events into single B2link data stream.

*should be REVO or REVO9 counter
**will be removed to increase bandwidth



Slow Control Path

- Routes slow control data to Data Concentrator, RPC Front-End, Scintillator Motherboard.
- Some Data Concentrator parameters are controlled by B2Link register interface (not shown).
- All scintillator and RPC parameters are sent using B2Link streaming interface.
- Routes data based on byte offset in serial file (packet).



RPC Slow Control

- The RPC Front-End board requires configuration values and (optionally) built-in-test control that is expected to be transmitted over each Belle2link:
  - Threshold value - 1248 values/Concentrator, 8-bits per value
  - Test pulser - 1248 built-in-test values/Concentrator, 1-bit per value
  - Test pulser control – some number of bits to turn test pulser on/off

Scintillator Slow Control

- The scintillator electronics require configuration values that are expected to be transmitted over each Belle2link
- Number of bKLM parameters if passed through Concentrator:
  - 300 MPPC channel bias voltage settings
  - 600 ASIC trigger threshold and DAC values
- Number of eKLM parameters if passed through Concentrator:
  - 1050 MPPC channel bias voltage settings
  - 2100 ASIC trigger threshold and DAC values

Remaining Issues (1)

The good:

1. Most of calibration happens on FEEs upon start
2. Data taking is possible up to 100 Hz trigger rate
3. Both scintillator and RPC hits are visible during local runs
4. Converging on fixing look-back parameter for scintillator in global runs

The bad:

1. Readout is slow
   - currently takes ~10ms per ROI if there is a hit → due to firmware implementation inefficiencies
2. Periodic TTLOST on KLM

The Ugly:

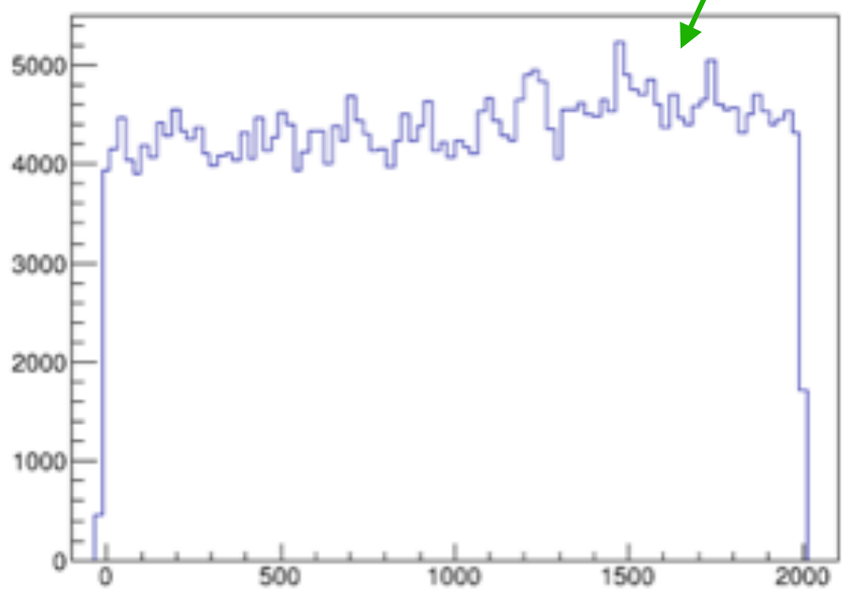
1. Some crates might have power/backplane issues
2. Still unclear if current trigger-timing coding is sufficient for UT3 operation

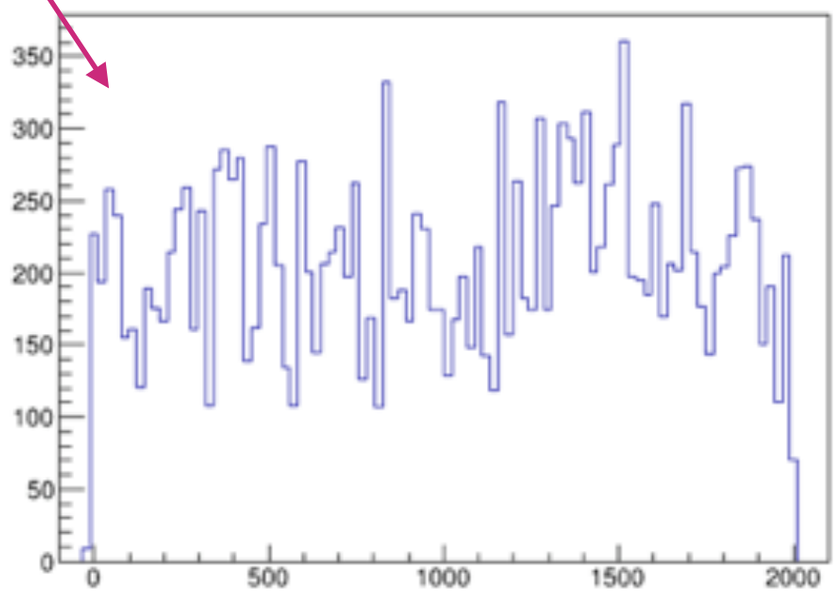
Remaining Issues (2)

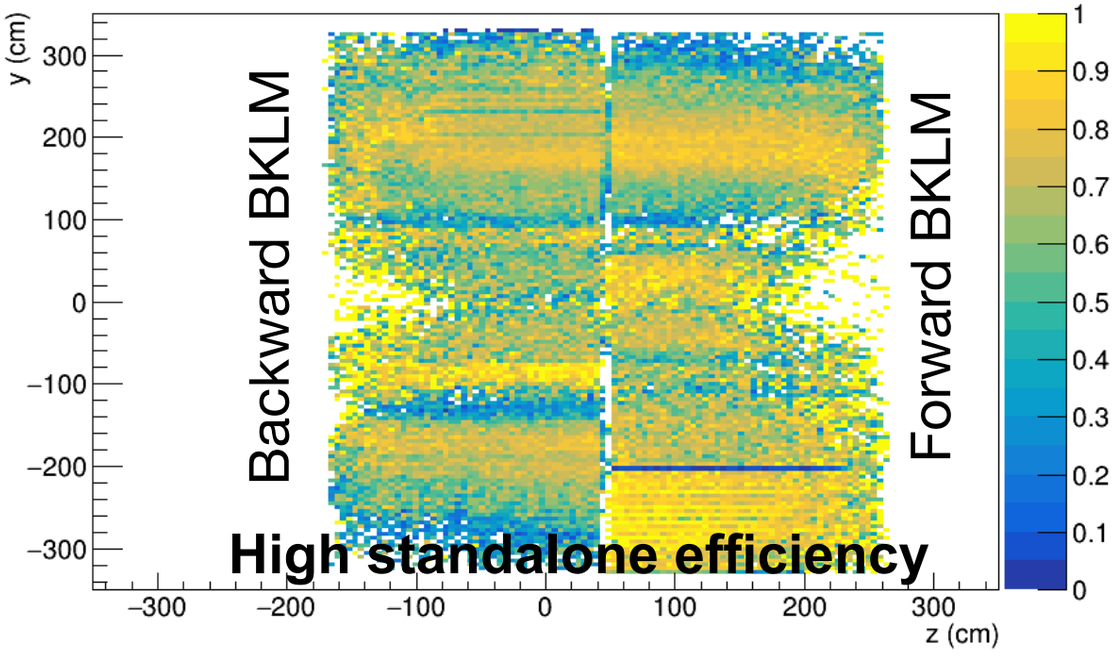
- Modify Scintillator Motherboard readout (Aurora Interface) to align DAQ readout so trigger data is aligned for time-ordering on Data Concentrator.
- Equalize the RPC and scintillator trigger data latency at the input of the time ordering logic on the Data Concentrator.
- Replicate the RPC event builder 13 times and remove the time-ordering logic to increase bandwidth, increase buffer size, and lower latency.
- Augment the fine-time (TDC) values with the REVO or REVO9 counter (instead of CTIME) for creation of GDL time stamp.

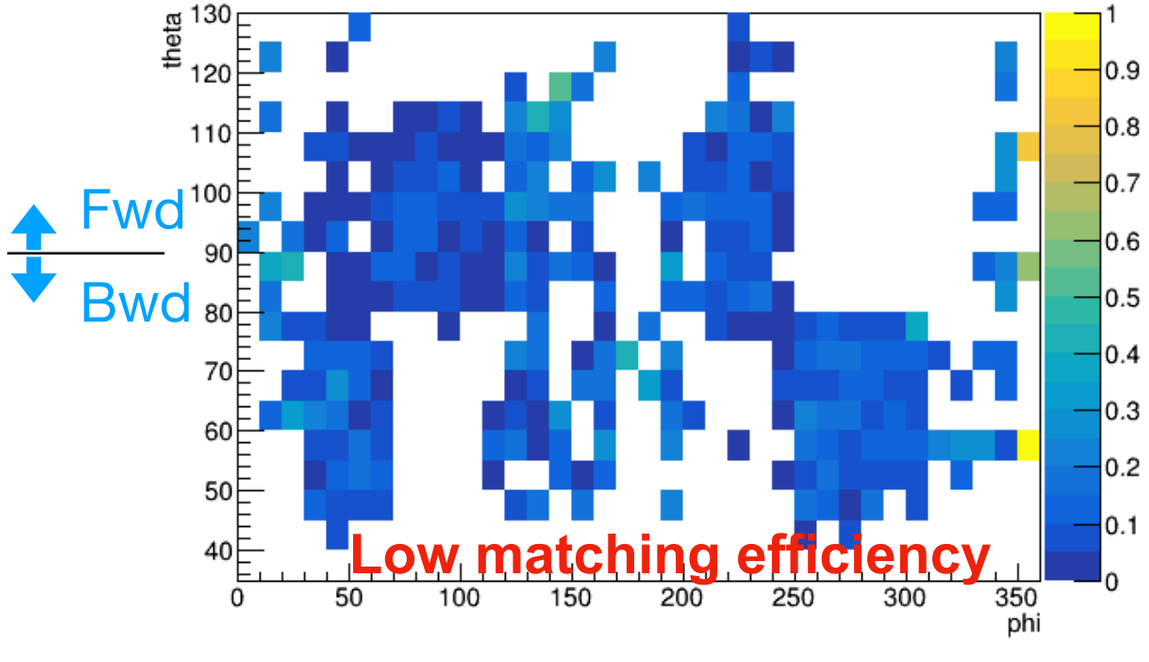
Timing & Efficiency in Global Cosmic Run

- No apparent trigger-coincidence peak in BKLM TDC histogram when selecting events with BKLM standalone tracks or with BKLM hits that match CDC tracks.









Moving Toward 30 kHz Readout

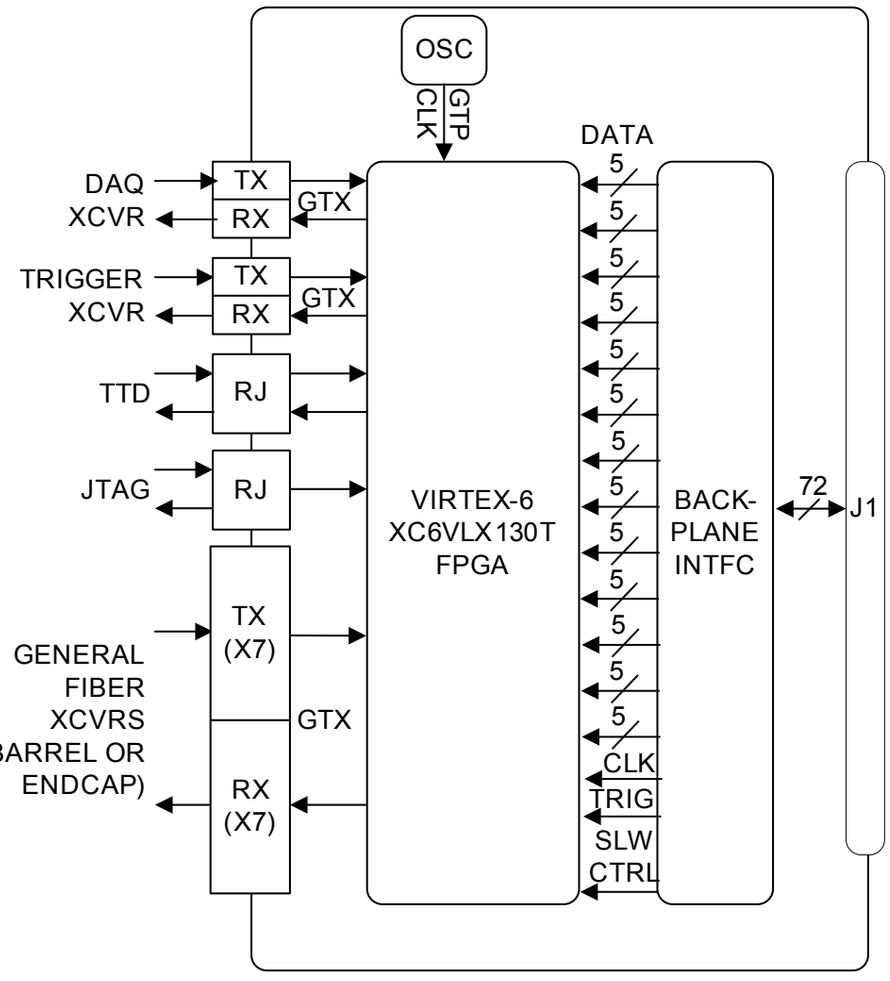
- **RPC readout is ready for 30 kHz readout today,** according to bench-test measurements at Indiana U
- Scintillator-readout firmware overhaul:
  - **Step 1: 100 Hz → 1 kHz: (Oct 2017)**
    - ✓ Increase internal FPGA clock from 64 to 127 MHz
    - ✓ Implement clock enables
    - ✓ Speed up digitization process in TARGETX readout sub-FW
  - **Step 2: 1 kHz → 10 kHz: (Dec 2017)**
    - ✓ Expand ROI readout to only channels of interest
    - ✓ Aggressive pedestal caching
  - **Step 3: 10 kHz → 30 kHz: (Jan 2018)**
    - ✓ Optimize readout process
    - ✓ Optimize/reduce readout window size/length

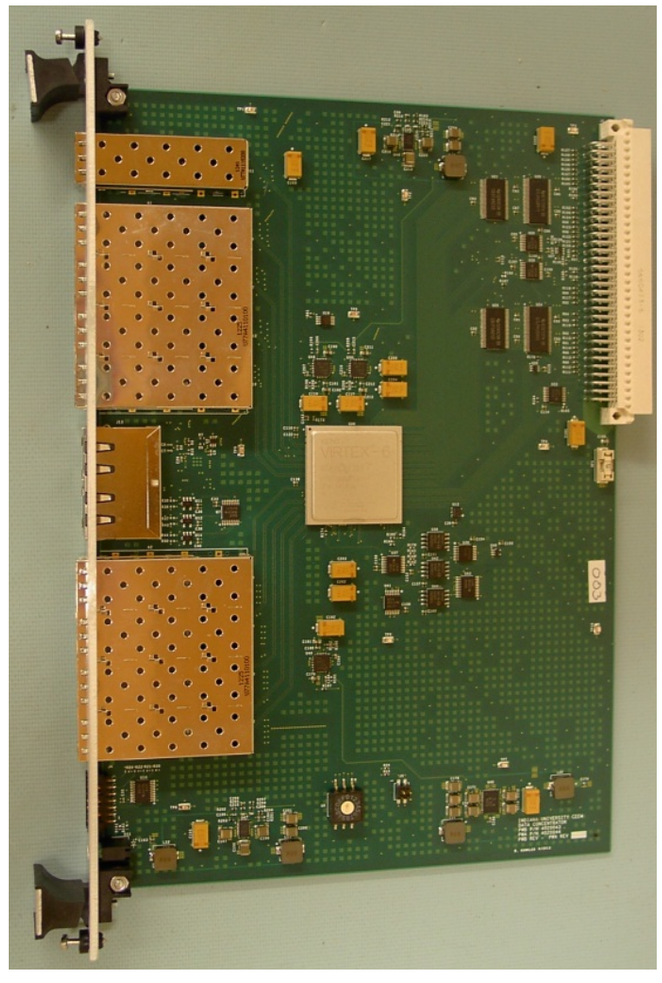
BACKUP

Data Concentrator Board

- Four Data Concentrator boards were manufactured on DOE funds.
- The boards were received 08/22/2013
- Remaining boards completed/installed in 2016.

- One timing and trigger distribution (TTD) interface.
- Transceivers for DAQ and trigger link
- Seven SFP transceivers used for data fiber link input from scintillator layers – 2 barrel or 7 endcap.
- Onboard clock for test without FTSW
- One Virtex-6 FPGA for data processing – scintillator coincidence, RPC time ordering, and RPC trigger window.





KLM Front End Electronics for Scintillator Readout

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