TOP Firmware Status & Plans

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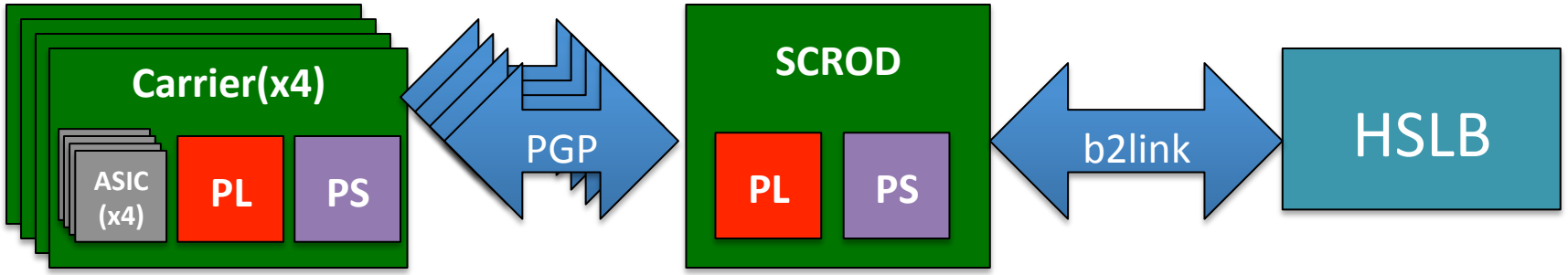
TOP Board Stack Architecture

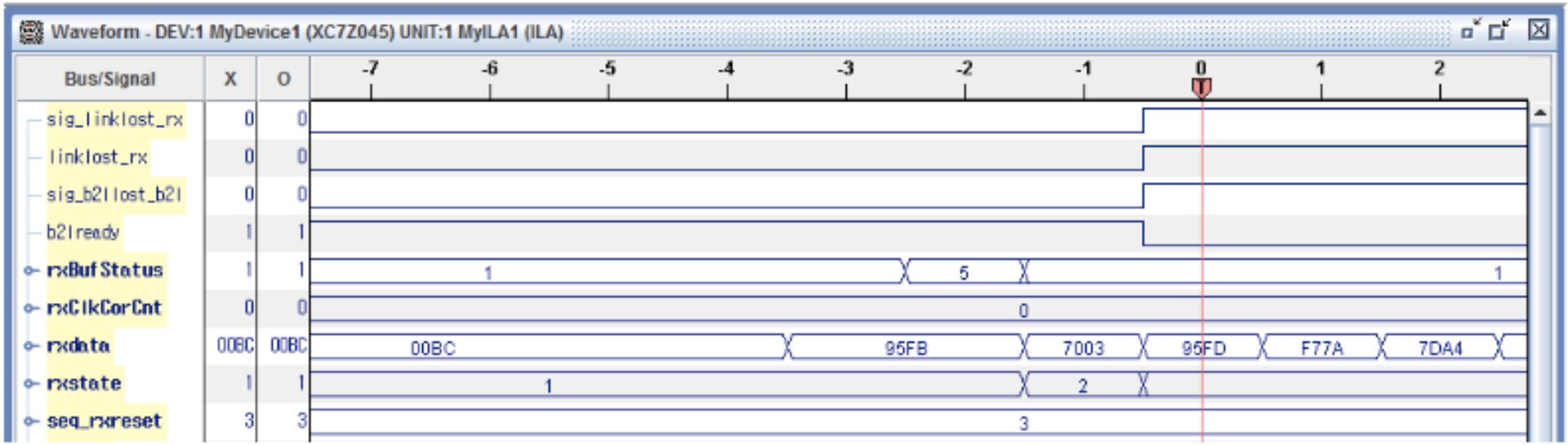
- Front-end modules utilize Zynq:
  - Kintex7 programmable logic [PL] +
  - ARM processing system [PS]



  - 4 total versions of “firmware”: SCROD/Carrier, PL/PS
  - GT links:
    - SCROD/Carrier links via PGP (custom protocol from SLAC).
    - SCROD/HSLB via b2link.
    - Trigger path via Aurora (see Nisar’s talk).

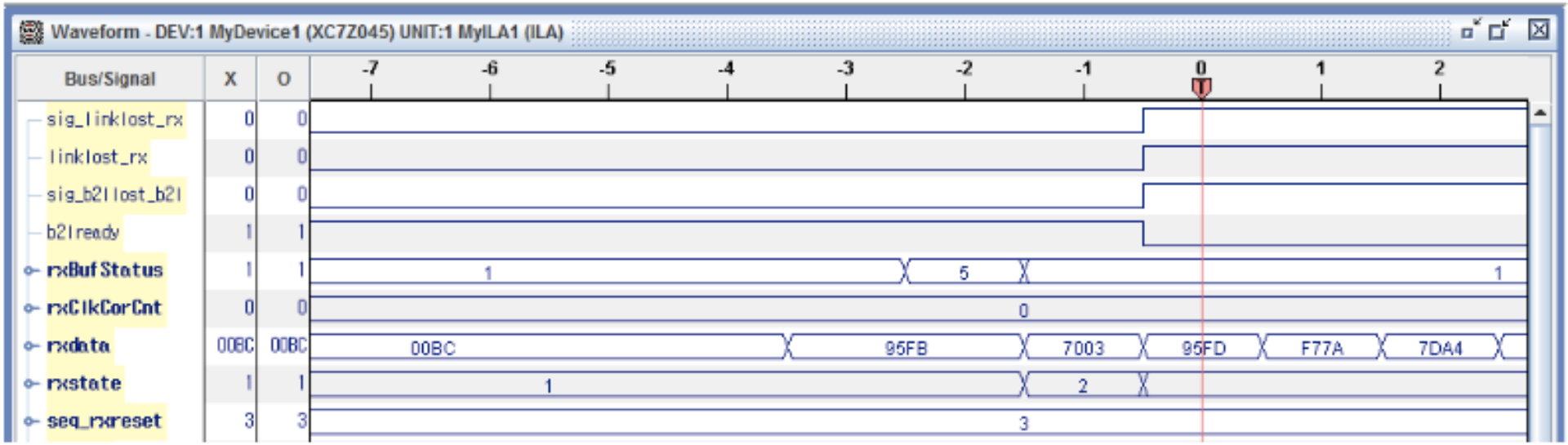
b2llost Issue(1)

- Since June(!), b2llost had been plaguing TOP.
  - This was declared top priority issue before moving forward with other high rate firmware features.
  - Linked to similar problem seen by Kyungho Kim in February.
  - Localized to an elastic buffer over/underflow in the GT.



b2llost Issue(2)

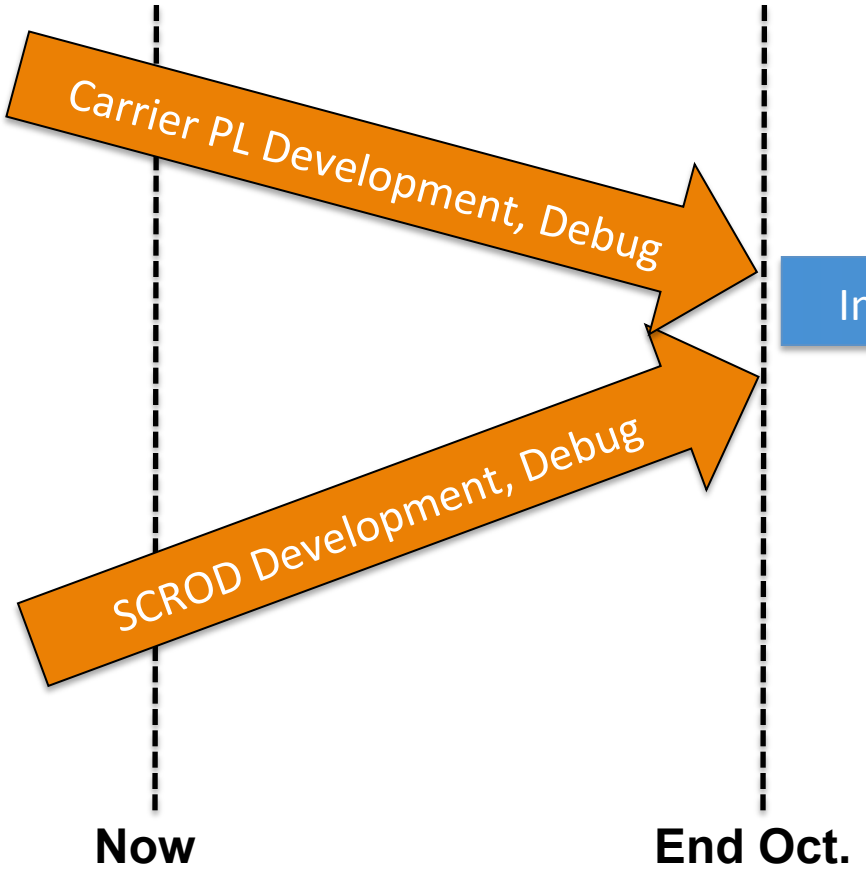
- Workarounds in SCROD, HSLB provided handling for repeated words (more in Nakao-san's b2link slides).
- Eventually solved... turned out to be a mis-set channel bonding port (if a GTX is set as a CB slave, it will not clock correct, even if CB is disabled in configuration settings).
- b2llost now seems resolved, investigating data corruption (not certain it's related).



Fast Readout (30 kHz)

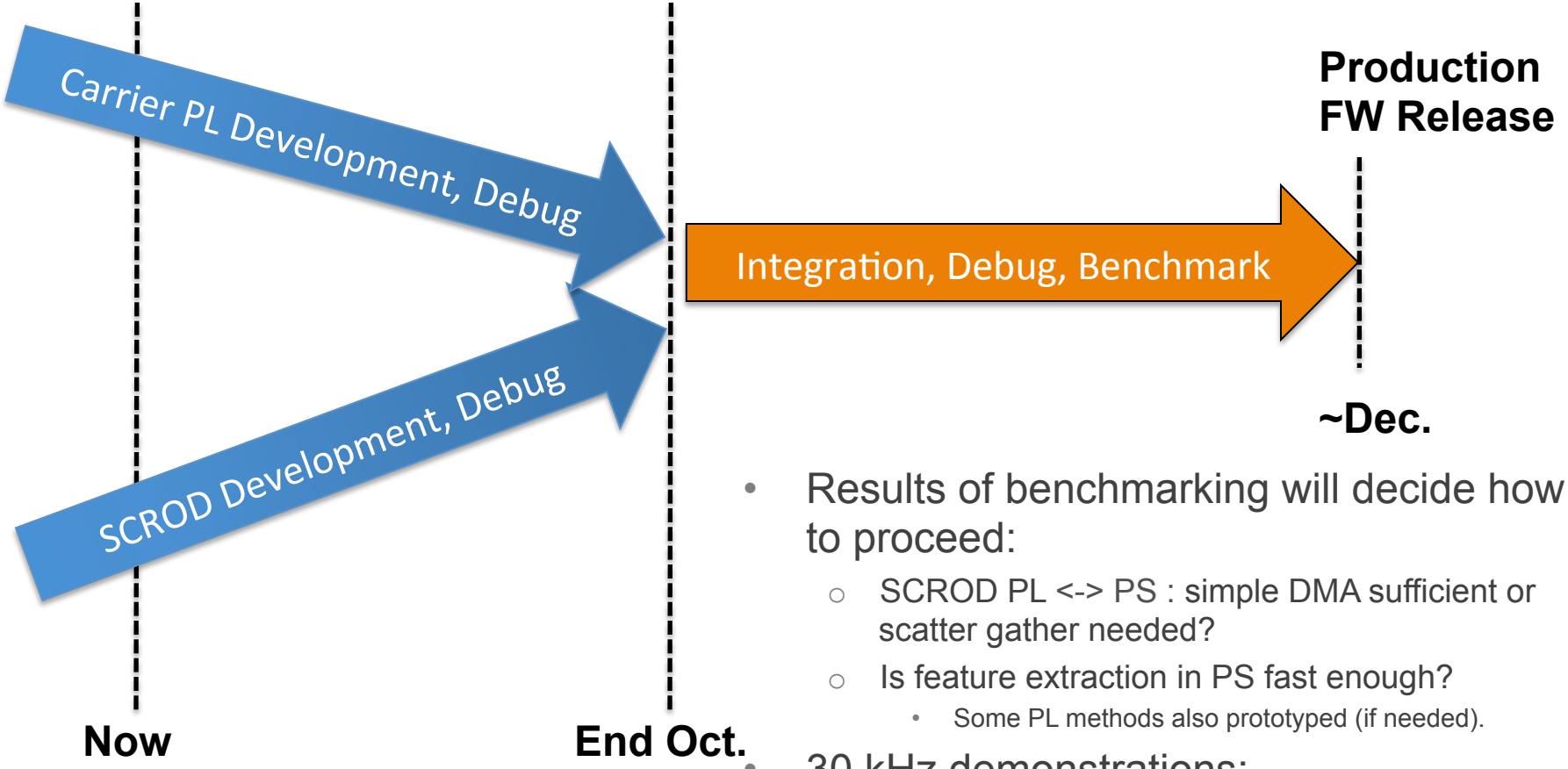
- Existing system is operating in “simple” mode.
  - Analog recording stops upon receipt of a trigger.
    - Each channel of each ASIC digitizes and reports 256 samples for every system trigger, resumes sampling only after digitization.
    - This is in obvious need of upgrade for high rate running.
  - Limited to ~750 Hz, as verified in local single module tests.
- A scheme has been developed to implement deadtime-less operation:
  - Implements simultaneous sampling and digitizing/readout.
  - Sends only data for channels with hits.
    - Even then, limits readout to 32 samples around the trigger.
  - Details available in Luca’s slides from TOP firmware bootcamp.
  - Split into two components:
    - Updated Carrier PL firmware to implement above.
    - Updated SCROD PL/PS to process new data stream.

Development Pathway (1)



- Carrier and SCROD development are underway in parallel.
  - Carrier PL – Luca M.
  - SCROD PL/PS – Kurtis N.
- Data formats have been developed for new deadtime-less protocol.
- Based on understanding of manpower constraints, targeting integration by end of October.

Development Pathway (2)



- Results of benchmarking will decide how to proceed:
  - SCROD PL <-> PS : simple DMA sufficient or scatter gather needed?
  - Is feature extraction in PS fast enough?
    - Some PL methods also prototyped (if needed).
- 30 kHz demonstrations:
  - Highly occupancy dependent.
  - Can make a simple demonstration that suppresses excess waveforms if needed.

Other Development Needs

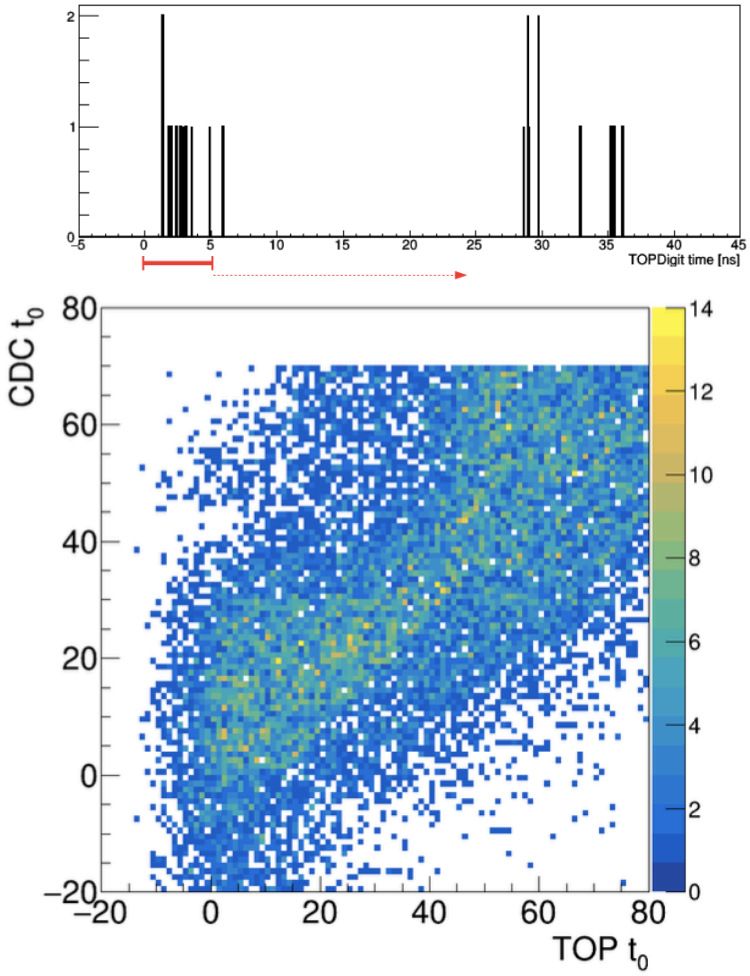
- At least two present known issues:
  - After b2llost resolution − data corruption.
    - Relatively new, still working to understand. Related to b2llost?
  - Inconsistent carrier firmware results − bad ASIC pedestals data.
    - Investigating under assumption of unconstrained in/output delays.
- Will continue to try to resolve these on existing firmware where possible.

  ➔ **We expect these issues are connected to exclusion of board stacks, and that those board stacks are recoverable (they've worked under certain firmware revisions!).**

- Many other lower priority additions/upgrades queued up.
  - See backup for details, full list maintained on Google Sheets.
  - Also some improvements to trigger path in Carrier PL.

t_0 Alignment: CDC vs. TOP

- Event t0 estimates between TOP and CDC have been studied by Ale Gaz in GCR data.
- TOP estimates come from a sliding window event-by-event.
  - Analysis is complicated by misalignment between board stack, for now calibrated with laser data. Production firmware aims to resolve this by design.
- CDC estimates come from **EventT0** in events with two back-to-back track segments.
- Correlated, but very broad!
- Checking our own unpacking...
- Would also like to coordinate with CDC to understand meaning of **EventT0** compared to TOP timing.

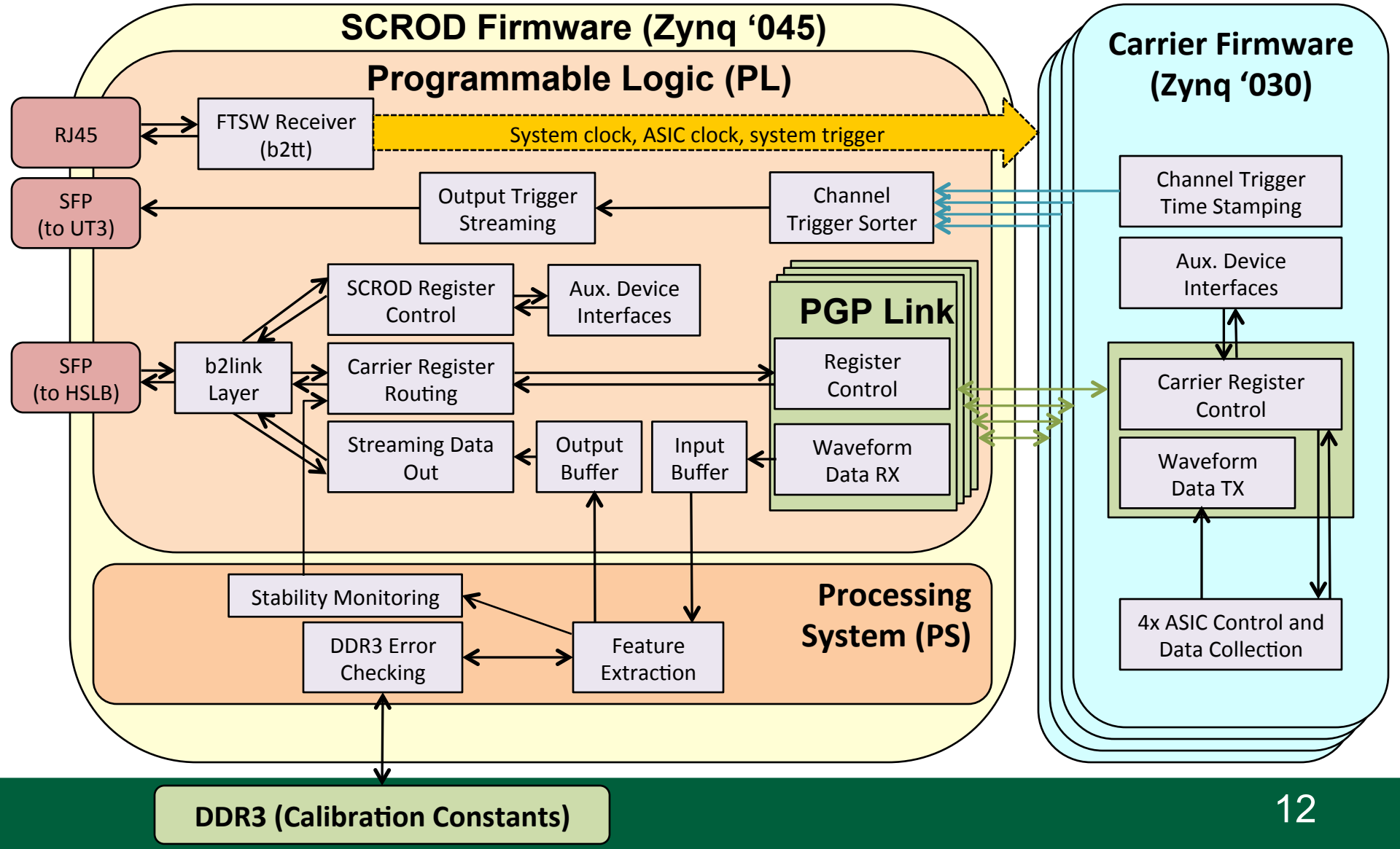


Major Milestones

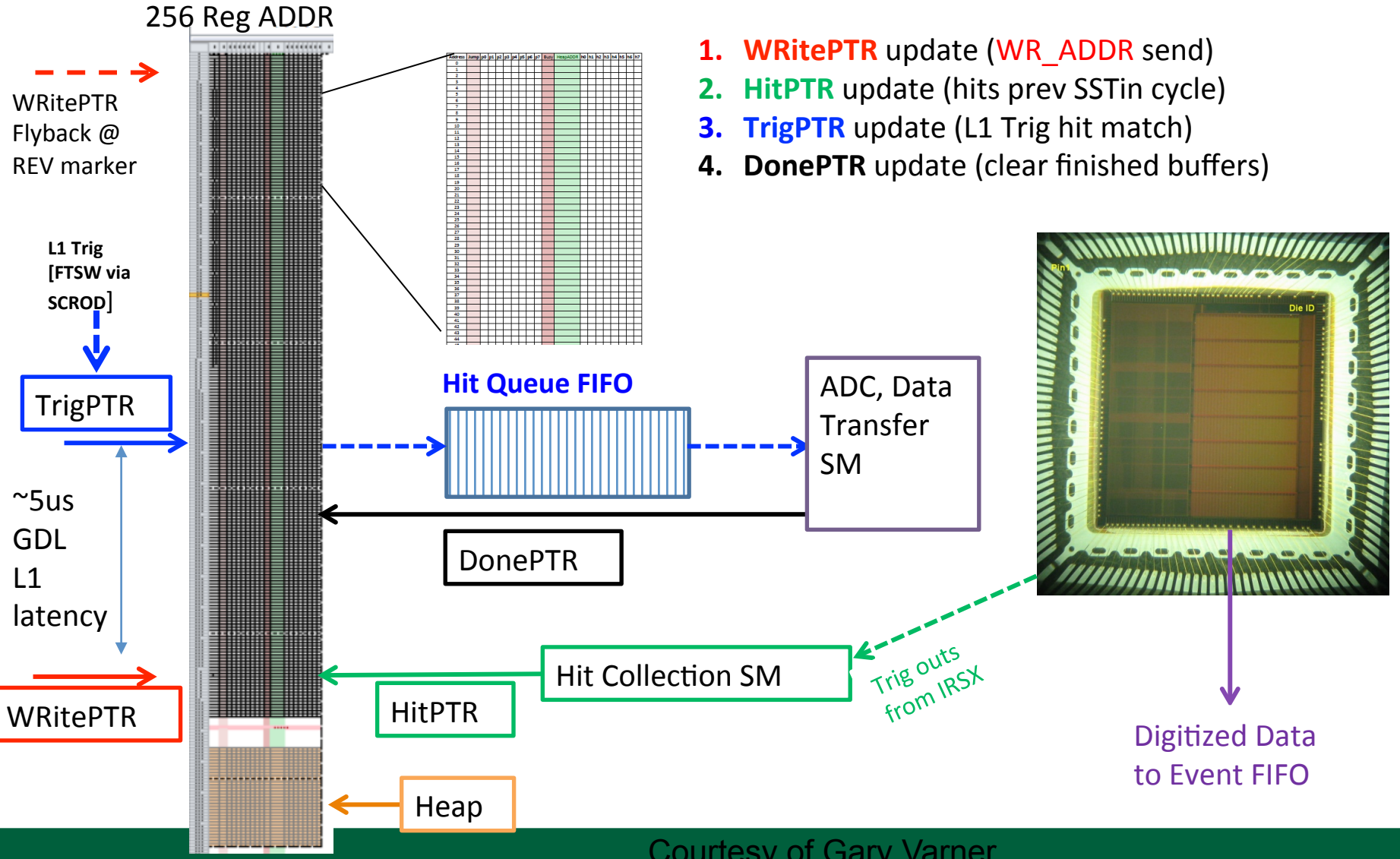
- Multi-hit readout carrier firmware.
  - Target: Oct. 31
- Multi-hit compatible SCROD PL/PS.
  - Target: Oct. 31
- Integrated multi-hit mode.
  - Target: Mid-Dec.
- Demonstration of 30 kHz operation.
  - Target: End-Dec.
    - Note: Could scale back to pseudo-30 kHz with event truncation if necessary.

Backup

Firmware Overview



MultiHit readout principle



1. **WRitePTR** update (WR_ADDR send)
2. **HitPTR** update (hits prev SSTin cycle)
3. **TrigPTR** update (L1 Trig hit match)
4. **DonePTR** update (clear finished buffers)

Courtesy of Gary Varner

Regaddr structure

Address	Jump	p0	p1	p2	p3	p4	p5	p6	p7	Busy	HeapADDR	h0	h1	h2	h3	h4	h5	h6	h7
0																			
1																			
2																			
3																			
4																			
5																			
6																			
7																			
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Jump = Address busy, go to Heap ADDR

P[0:n] hit bits collection

Busy = Heap ADDR trigger matched, can no longer accept hits

HeapADDR = Heap WR_ADDR sent

H[0:n] hit bits for Heap ADDR

Courtesy of Gary Varner

Overall Task List

Epoch	Task ID	Description	Component	Assigned to	Target Deadline	Status
	A1	Production SCROD release 1.0 (post GCR/pre Phase II)	SCROD PL, PS	Kurtis	21 Sept	continue Module debug post GCR run
Post GCR	A2	Production Carrier release 1.0 (post GCR/pre Phase II)	Carrier PL	Luca M.	21 Sept	continue Module debug post GCR run
High priority	B1	b2llost debug registers	SCROD PL	Lynn	ASAP	Under debug test
(now!)	B2	Multicast PS programming!	Carrier PS	Needed!	ASAP	Huge bottleneck in current startup
	B3	Benchmark PS pedestal subtract and CFD	SCROD PS		ASAP	
	B4	Benchmark IRSX digitization and readout	Carrier PL		ASAP	
	B5	Configure Carrier Registers, IRSX	Carrier PS		ASAP	automate at start-up (replace b2link config)
	B6	Configure SCROD Registers	SCROD PS		ASAP	automate at start-up (replace b2link config)
Pre-	C0	Module specific tuning	All		Dec. 1	DDR parameter tuning
Phase II	C1	Verify SCROD PL CFD	SCROD PL		Oct. 1	Hand off from Tobias? -- almost done
(end 2017)	C2	Implement SCROD PL Template fitter	SCROD PL		Dec. 15	Follow-on from Task C1
	C3	Support new Belle2Link iTOP packet format	SCROD PS			
	C4	Remove CFD calculation from PS	SCROD PS			
	C5	Status registers for all FIFO under/overflow bits	Carrier+SCROD PL			
	C6	Wire up remaining registers and remove unused ones	Carrier+SCROD PL			
	C7	Move Pedestal subtraction to the carriers PS?	SCROD PS			Fallback is do on SCROD, needs D3
	D1	Code Re-write	Carrier+SCROD PS			more/smaller *.h files, cleanup of defns, data structs
	D2	Expand/improve slow data	SCROD PS			
	D3	Support pedestal prefetch (if needed)	SCROD PS			
	D4	PMT Integrated Charge scalers (non-rollover)	Carrier PL			
		Support use of second core ?	SCROD PS			
		Revisit and rework FSMs	SCROD PL			

Critical tasks: B2, B5-6 (speed start-up)
C1,C2 (30kHz L1 trigger)
C0 (full detector operation)

Many others are less time critical

Continued Task List

19		C7	Move Pedestal subtraction to the carriers PS?	SCROD PS		Fallback is do on SCROD, needs D3
20						
21		D1	Code Re-write	Carrier+SCROD PS		more\smaller *.h files, cleanup of defns, data structs
22		D2	Expand/improve slow data	SCROD PS		
23		D3	Support pedestal prefetch (if needed)	SCROD PS		
24		D4	PMT Integrated Charge scalers (non-rollover)	Carrier PL		
25		D5	Fix test benches	All		Many checked in svn, but never updated
26			Support use of second core ?	SCROD PS		
27			Revisit and rework FSMs	SCROD PL		
28			Rewrite of B2linkFrontEnd/B2Data/B2LinktoAXI	SCROD PL		
29						
30			AxiCommon/AxiVersion cleanup	Carrier+SCROD PL		
31			Fix the broken registers	Carrier+SCROD PL		
32						
33			Define and enforce code style!	SCROD PL		VHDL
34			Define and enforce code style!	SCROD PS		Software
35			Define and enforce code style!	Carrier PL		VHDL
36			Define and enforce code style!	Carrier PS		Software

Many are good student or first "FW" projects (especially on PS – all in C code)

List will continue to evolve, so even if don't have time now, if do at some point, please let us know