



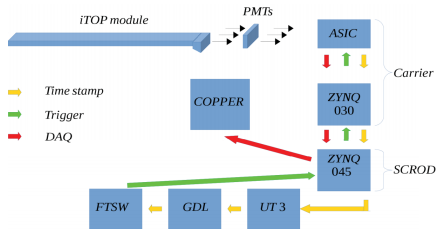
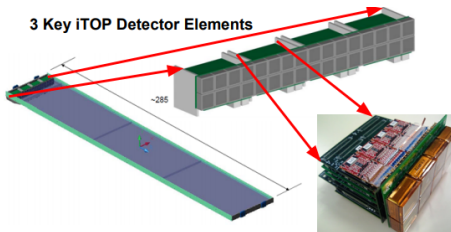
TOP Trigger Status

Nisar Nellikunnummel
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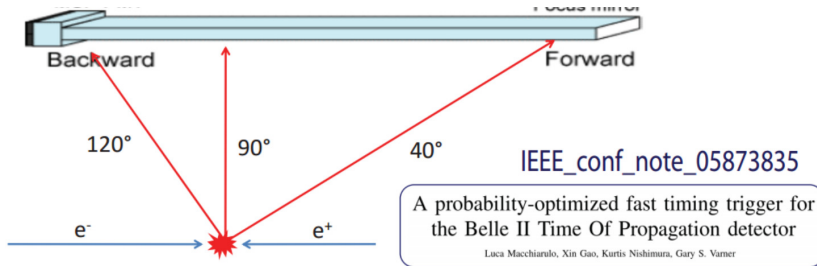
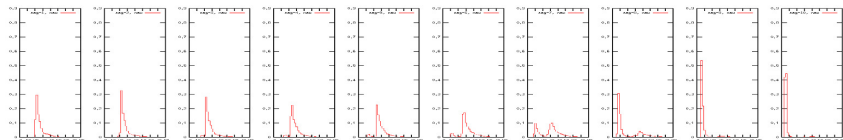
University of Pittsburgh

August 23, 2017

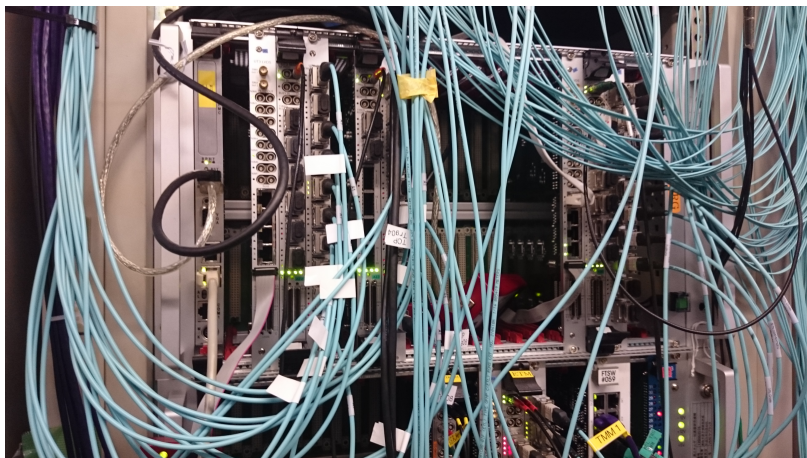
- TOP counter is designed for barrel particle identification
- Its good intrinsic time resolution enables t_0 (time of arrival of charged particles on TOP) estimation with ns time resolution
- This t_0 helps to reduce data volume of out-of-time hits in SVD



- Timestamps: Time of arrival of photons on PMT
- Photons (timestamps) produced from a charged particle follow some pattern based on the location of hit on the bar

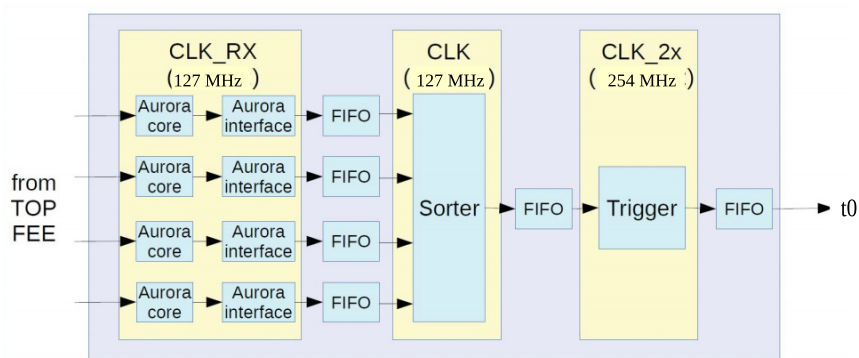


Setup at KEK



- Timestamps are produced on FEE and send to UT3 using AURORA 8b10b protocol at a line rate 5.08Gbps.
- Timestamping is based on revo9 marker synchronized with the accelerator clock
- revo9 marker is updated every 90us
- Timestamp is represented by the number of clock cycles since most recent revo9 marker
- Clock used for timestamps allows 3ns binning. Therefore 16 bits are sufficient for timestamping (timestamping is done on both edges of axiClk(169 MHz).
 $\text{axiClk} = 8 \times \text{SSTClk} = 8 \times \text{FTSWClk}/6$, $\text{FTSWClk} = 127 \text{ MHz}$)
- Timestamping at 1ns binning will improve trigger performance

t_0 s are estimated separately on each TOP bar and are combined later

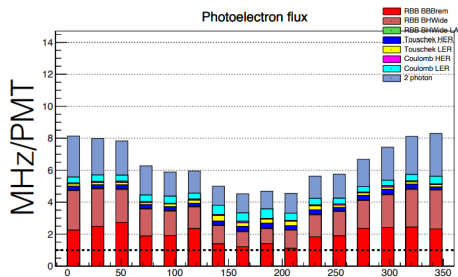


- 1 Receive: Timestamps come through 4 channels from FEE
- 2 Sorting: 4 channels are merged and Timestamps are sorted according to time
- 3 Trigger: t_0 is estimated by fitting the Timestamps to PDFs by a Maximum Likelihood Fitting

- Photon Flux significantly above desired levels

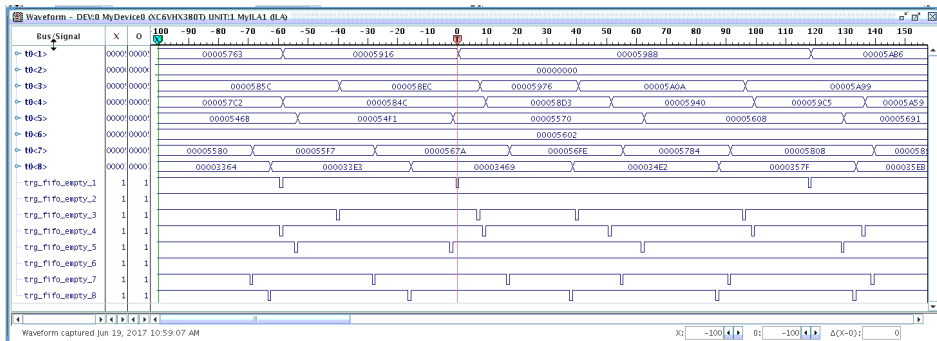
Beam Background

- 1 8 MHz/PMT
- 2 64 MHz/Board Stack
- 3 256 MHz/TOP Bar



T. Nanut, 27th B2GM (June 21, 2017)

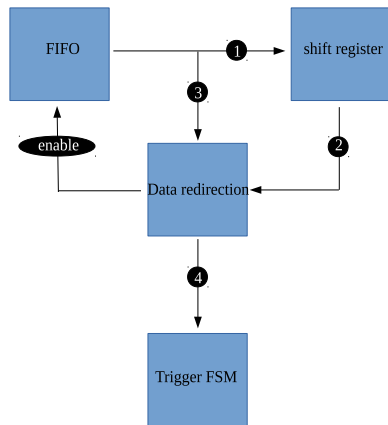
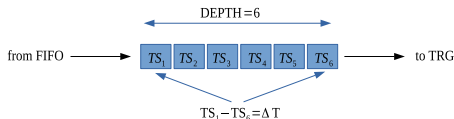
t0s in presence of Background (electronic noise)



- Triggers are too frequent in presence of background since every timestamp arrive at UT3 are processed
- This problem is already known from a software simulation
- Possible solution: Run Trigger algorithm only during the arrival of timestamps belong to a signal

Instantaneous Hit Time Density (IHTD)

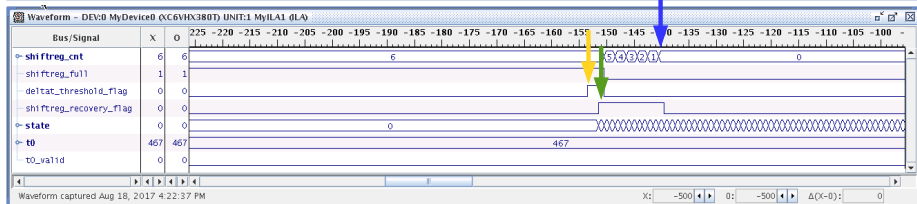
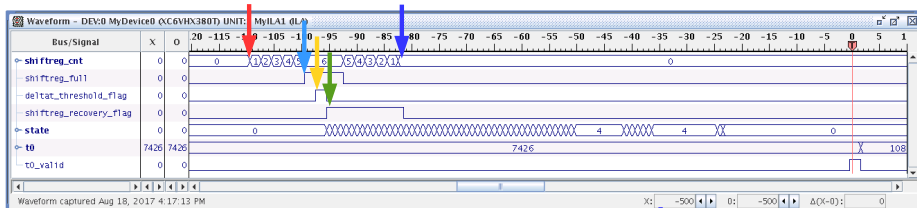
- Initially, TSs go to "Shift register" and continuously monitored by "Data redirection" (path 1)
- whenever $\Delta T < \text{THRESHOLD}$
 - Stop taking TSs from FIFO
 - Recover the 6 TS which is already in Shift reg.(path 2& 4)
- Continue to take TSs from FIFO, after recovering 6 TS in shift reg. (path 3& 4)



- Signal identification efficiency should be maximized by optimizing THRESHOLD and DEPTH

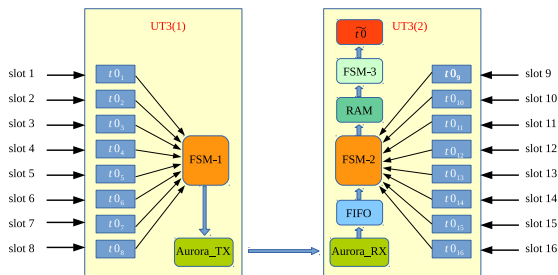
Firmware with IHTD

- 1 shiftreg_cnt
- 2 shiftreg_full
- 3 deltat_threshold_flag
- 4 shiftreg_recovery_flag

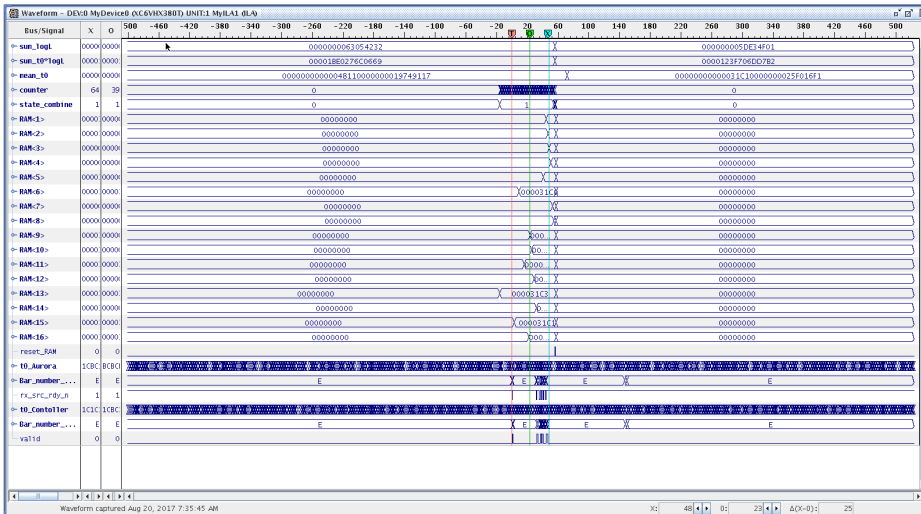


$$\tilde{t}_0 = \frac{\left(\sum_{i=1}^{i=16} t_{0_i} L_i\right)}{\left(\sum_{i=1}^{i=16} L_i\right)}$$

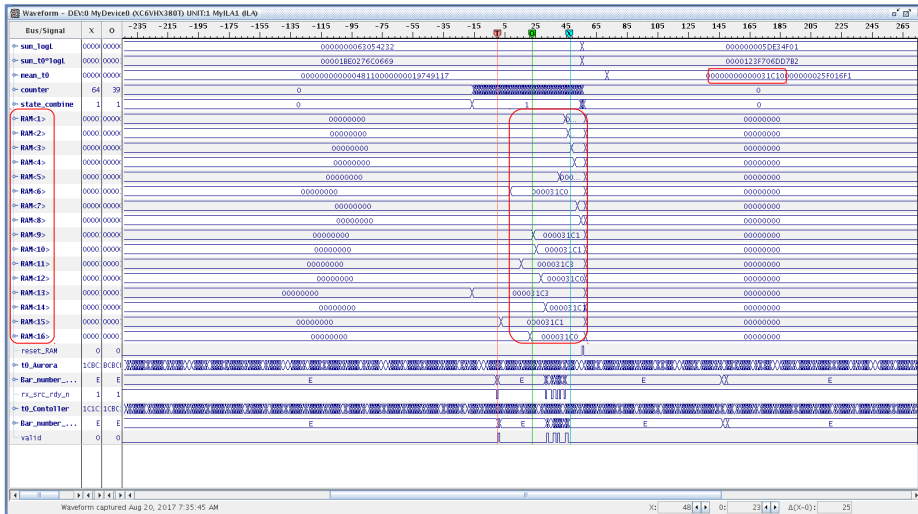
- t_{0_1} - t_{0_8} on UT3(1) and t_{0_9} - $t_{0_{16}}$ on UT3(2)
- All t_0 s on UT3(1) are send to UT3(2) (4-lane AURORA with each lane is 5.08 Gbps)
- All t_0 s are temporarily stored on a RAM until \tilde{t}_0 is estimated



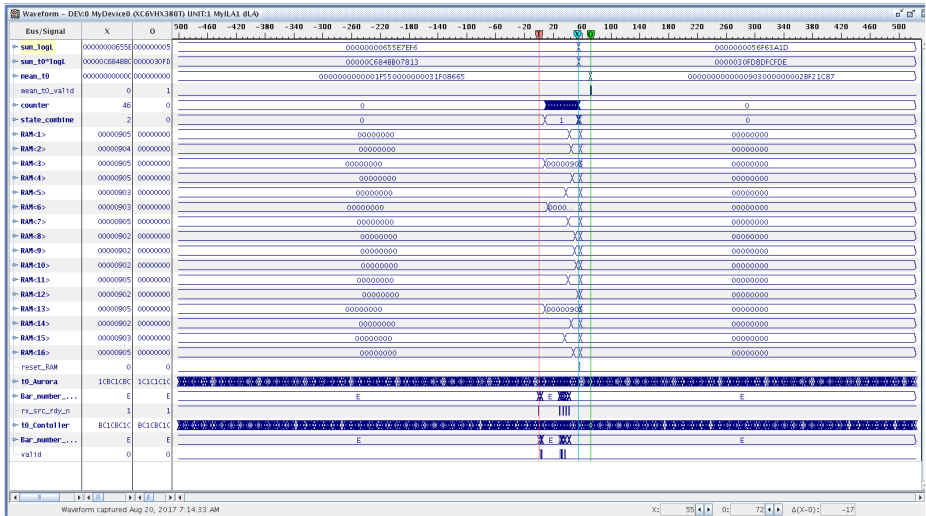
Combined t0 on UT3(2)



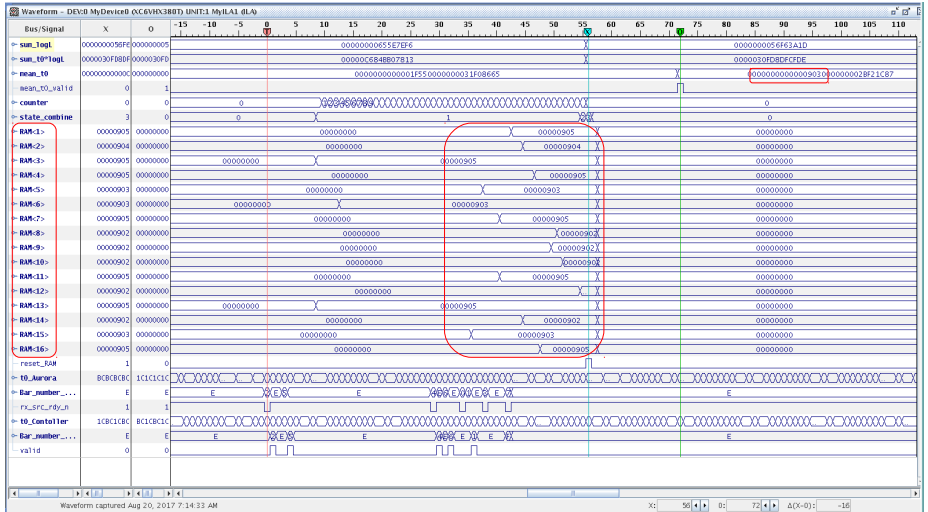
Combined t0 on UT3(2)

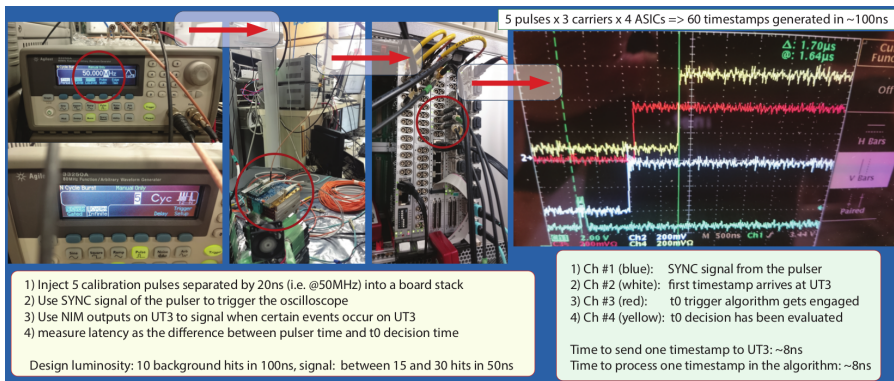


Combined t0 on UT3(2) (latency added)



Combined t0 on UT3(2) (latency added)





- Latency estimated for single Bar by injecting calibration pulses in to FEE
- Latency depends on number of hits and have contribution from AURORA, XILINX cores used for weighted sum of t0 etc.
- Overall expected latency below 2.5 us

- Timestamping is implemented in all latest FEE FW and reliably transmitting them to UT3 at 5.08 Gbps
- The algorithms for collecting and combining t0 decisions from individual bars have been designed and tested at KEK
- TOP Trigger latency is measured and the value is well within maximum allowed limit
- TOP Trigger FW with Instantaneous Hit Time Density (IHTD) is designed and tested at Pittsburgh. Working on optimization of various parameters to get best possible performance of Trigger FW.
- Soon start working on interface to GDL.