3D tracker firmware

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Review

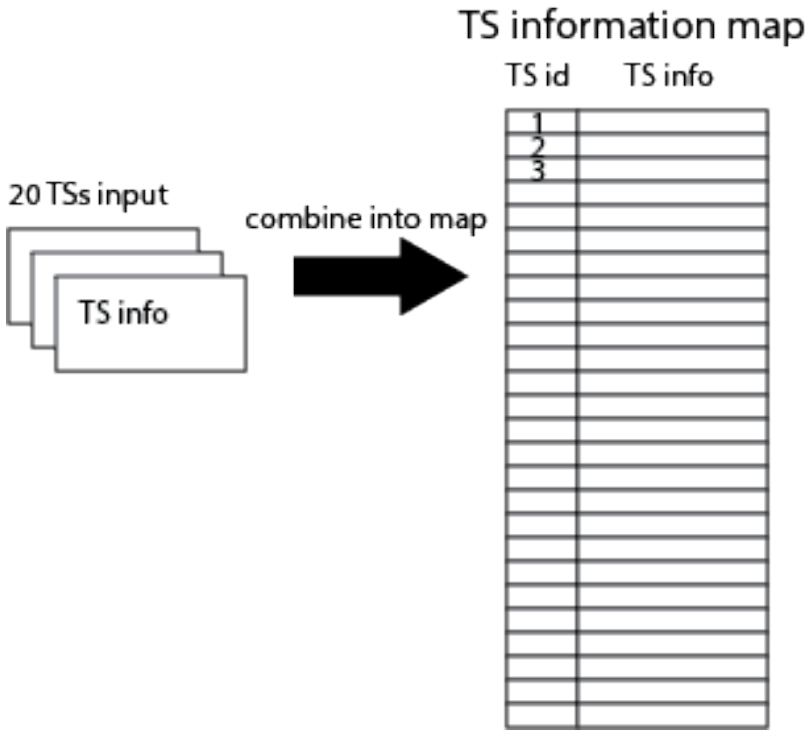
- Could not make firmware. Timing constraint error.

UT3_2D Project Status (08/21/2017 - 22:29:41)			
Project File:	UT3_2D.xise	**Parser Errors:**	No Errors
Module Name:	UT3_2D	**Implementation State:**	Placed and Routed
Target Device:	xc6vhx565t-2ff1923	• **Errors:**	No Errors
Product Version:	ISE 14.7	• **Warnings:**	3692 Warnings (3692 new)
Design Goal:	Timing Performance	• **Routing Results:**	All Signals Completely Routed
Design Strategy:	SmartXplorer - mapioreg	• **Timing Constraints:**	X 1 Failing Constraint
Environment:	System Settings	• **Final Timing Score:**	322 (Timing Report)

Number of Slice Registers	49,192	708,480	6%
Number used as Flip Flops	49,191		
Number used as Latches	1		
Number used as Latch-thrus	0		
Number used as AND/OR logics	0		
Number of Slice LUTs	110,602	354,240	31%
Number used as logic	98,572	354,240	27%
Number using O6 output only	94,205		
Number using O5 output only	2,963		
Number using O5 and O6	1,404		
Number used as ROM	0		
Number used as Memory	9,679	101,920	9%
Number used as Dual Port RAM	0		
Number used as Single Port RAM	128		
Number using O6 output only	128		
Number using O5 output only	0		
Number using O5 and O6	0		
Number used as Shift Register	9,551		
Number using O6 output only	9,141		
Number using O5 output only	0		
Number using O5 and O6	410		
Number used exclusively as route-thrus	2,351		
Number with same-slice register load	2,220		
Number with same-slice carry load	131		
Number with other load	0		

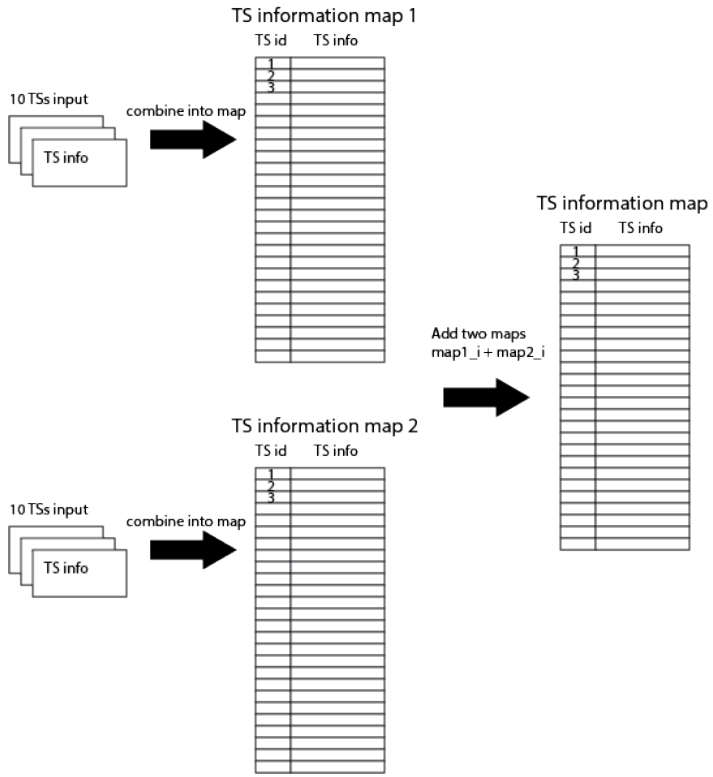
Solving timing constraint problem

- VHDL was modified to solve the timing constraint error.
- The timing constraint path was from the input unpacker.
  - Happens when combining information.



Solving timing constraint problem

- The method to combine information was modified to fix the timing constraint.
  - Combine information in two steps.
  - Use add operator to combine information.



Solving timing constraint problem

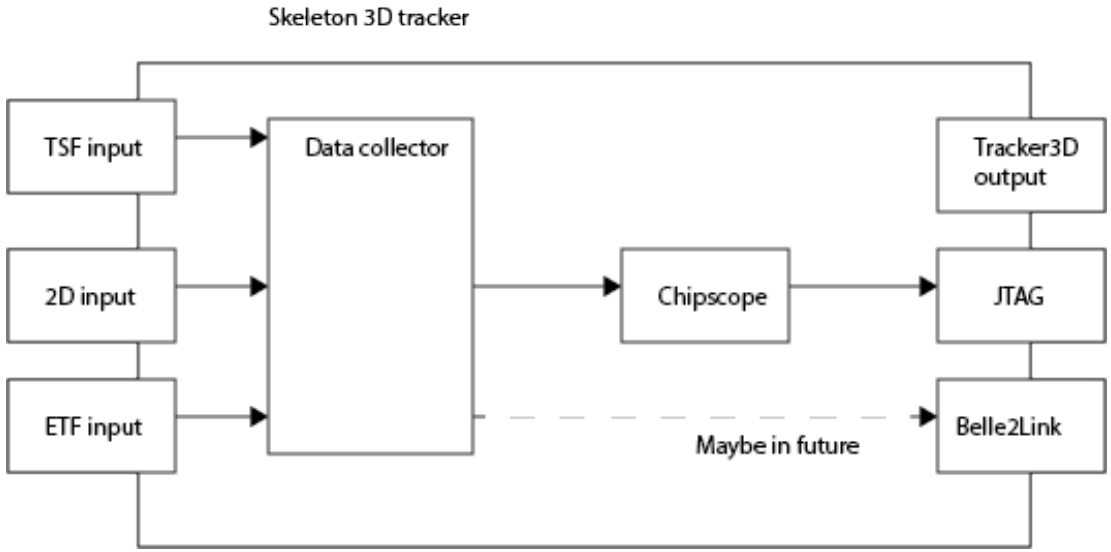
- The timing constraint problem was fixed.

UT3_2D Project Status (07/04/2017 - 08:48:56)			
Project File:	UT3_2D.xise	**Parser Errors:**	No Errors
Module Name:	UT3_2D	**Implementation State:**	Placed and Routed
Target Device:	xc6vhx565t-2ff1923	• **Errors:**	No Errors
Product Version:	ISE 14.7	• **Warnings:**	4539 Warnings (51 new)
Design Goal:	Timing Performance	• **Routing Results:**	All Signals Completely Routed
Design Strategy:	SmartXplorer - maplogoptregdup	• **Timing Constraints:**	All Constraints Met
Environment:	System Settings	• **Final Timing Score:**	0 (Timing Report)

Number of Slice Registers	91,966	708,480	12%
Number used as Flip Flops	91,963		
Number used as Latches	1		
Number used as Latch-thrus	0		
Number used as AND/OR logics	2		
Number of Slice LUTs	178,363	354,240	50%
Number used as logic	165,689	354,240	46%
Number using O6 output only	161,327		
Number using O5 output only	2,956		
Number using O5 and O6	1,406		
Number used as ROM	0		
Number used as Memory	10,261	101,920	10%
Number used as Dual Port RAM	0		
Number used as Single Port RAM	128		
Number using O6 output only	128		
Number using O5 output only	0		
Number using O5 and O6	0		
Number used as Shift Register	10,133		
Number using O6 output only	9,942		
Number using O5 output only	0		
Number using O5 and O6	191		
Number used exclusively as route-thrus	2,413		
Number with same-slice register load	2,281		
Number with same-slice carry load	132		
Number with other load	0		

Skeleton 3D firmware

- A skeleton 3D firmware was made.
  - Only purpose is to record input data to the 3D firmware.
  - Currently uses Chipscope to record the data.



Plans

- During September
  - Record data using the skeleton 3D firmware.
  - Add the 2D fitter to the 3D tracker. (Make firmware)
- During October
  - Debug the 3D tracker.

Summary

- The timing constraint problem was solved.
- A skeleton 3D firmware was made.
- Plan to make full 3D tracker firmware by September.

Backup